# FIXED AND RECONFIGURABLE, FULLY INTEGRATED, SWITCHING POWER SUPPLIES FOR DYNAMIC LOADS

A Dissertation

Presented to the Faculty of the Graduate School

of Cornell University

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

Waclaw Godycki

August 2014

FIXED AND RECONFIGURABLE, FULLY INTEGRATED, SWITCHING POWER SUPPLIES FOR DYNAMIC LOADS

Waclaw Godycki, Ph.D.

Cornell University 2014

The ever present trend to provide faster computation for less power has been one of the most important drivers of the semiconductor industry. From device engineering where balancing dynamic and leakage power is the key tradeoff, to high-level operating system task scheduling, the goal is always to increase efficiency without sacrificing performance. The recent shift to multicore processors makes the power optimization of the system more relevant than ever. In addition, attempts to bring voltage regulation on chip allow for dynamical power management on short time scales not possible before. This work explores the challenging design space of fully integrated, step-down voltage conversion and regulation. To reduce complexity and area overheads, one approach is to group cores (loads) in independent voltage domains and power them with a relatively large, inductor-based converter. To this end, a 3-level buck-type design is presented with efficiency improvements at low current loads to enable efficient operation in extended sleep states. To achieve per-core supply voltage control, relatively small switched capacitor converters are explored. Considered individually, these converters need to be over-provisioned for the worst case load scenario. However, substantial area savings can be achieved by dynamically reallocating capacitance to supply power to the most demanding cores/loads. In addition to 40% area savings, further exploration reveals order of magnitude

better transient response and better efficiency at low power for these Reconfigurable Power Distribution Networks.

# Biographical Sketch

Waclaw (Wacek) Godycki was born in Katowice, Poland. He attended elementary school in his native Ustron, Poland. He graduated from LOTE high school in Cieszyn. He attended Columbia University form 2000-2004 where he obtained his undergraduate degree in Bachelor of Science in Electrical Engineering. Upon graduation he joined Analog Devices Inc. in Boston, MA. He worked in Advanced Process R&D group on 1/f noise measurement and modeling and also on improving the quality factor of inductors through process modifications. In 2008, he started to work towards his Ph.D. degree at Cornell University. Early on, he investigated nonlinear Teager-Kaiser operator for UWB radio applications. He also designed high precision, Incremental Sigma-Delta Converters before switching focus to fully-integrated power supplies. In 2014 he accepted a position at Eridan Communications in Santa Clara, CA to work on RF Power Amplifiers.

I would like to dedicate this work to parents, Drogomira and Andrzej Godycki, for their never ending and complete support in any and all endeavors in my life and to my loving fiancee, Paula Petrica.

# Acknowledgements

I would like to thank my adviser Dr. Alyssa Apsel for guidance along the difficult path of obtaining an advanced degree and spirited discussions. I am grateful to my committee members Dr. Christopher Batten and Dr. David L. Hysell for asking the fundamental questions that are often the hardest the answer, but also the most insightful. I have learned a lot from both of you in terms of knowledge, but also in how to approach problems in a more systematic and scientific way.

I would like to thank my lab mates who have graduated or are graduating soon, from whom I have learned a great amount of practical knowledge especially during my first years in graduate school.

I took my first steps as an engineer under supervision of ADI fellow Jake Steigerwald and then fellow Susan Feindt, both of whom proved to be great mentors. Thank you for your guidance over those years.

# Table of Contents

# Chapter 1

# Introduction

Traditionally, DC-DC step-down converters were used to convert the noisy higher voltage supply available from the system's environment (e.g., solar cell, battery, wall socket) into the multiple voltage levels required by the system. They are usually based on efficient switch-mode circuits that use either inductors or capacitors as energy storage elements. These regulators have traditionally been implemented off-chip for two key reasons: (1) limited availability of high-breakdown voltage transistors in high-performance logic processes; and (2) limited availability of integrated energy-storage elements with suitable energy densities. They are typically implemented as buck converters that can utilize large inductors and capacitors available off-chip, which in turn allows them to achieve efficiencies of around 90% even for a few volts of step-down voltage. They also employ a feedback loop to provide regulation of the output voltage as the load current demand changes.

Monolithic integration using a standard CMOS process provides a tremendous cost incentive that has long motivated system designers across the computing stack to include more functionality within a single chip. This system-on-chip (SoC) integration enables low-power embedded platforms to include a

diverse array of components such as processing engines, accelerators, graphics processors, embedded flash memories, external peripheral interfaces, small-signal RF circuitry, and analog-to-digital/ digital-to-analog converters. Almost every computing system requires closed-loop voltage regulators that, at first glance, seem like another likely target for monolithic integration. However, the economic pressure towards monolithic integration has simply not been enough to overcome the loss of efficiency coincident with using on-chip voltage regulation.

Recent technology trends suggest that we are entering a new era where it is now becoming feasible to reduce system cost by integrating switching regulators on-chip. High-speed switching efficiencies have increased with technology scaling, reducing the need for very high-density inductors and capacitors. This trend is evident in industry, especially in Intel's recent Haswell microprocessors which use in-package inductors with on-chip regulators to provide fast changing supply voltages for different chip modules [21,33]. At the same time, materials improvements such as integrated in-package magnetic materials (e.g., Ni-Fe [45]) and new integrated on-chip capacitor organizations (e.g., deep-trench capacitors [3, 8]) have improved the density of the energy storage elements that are available.

## 1.1 Chip Power Requirements with Scaling Supply Voltages

Developments in deep sub-micron technologies resulted not only in faster computation, but also in a reduction in energy per operation. Improvements in transistor performance were possible by thinner gate oxides and lower threshold voltages. This resulted in scaling of the supply voltages from 5V two decades

ago to 1V or less. The low supply voltages, combined with increased power densities due to faster clocks and more tightly packed transistors place an increased burden on the power delivery to the chip. For a given amount of power dissipated by the chip, a reduction in voltage results in a proportional increase in current. Each of the supply and ground pins has inductance and resistance associated with it causing dI/dt and IR related fluctuations during sudden changes in load current demands. There are two ways to mitigate this effect: increase the number of supply and ground pins or increase the amount of on-chip decoupling capacitance [18]. Unfortunately, both of these approaches directly relate to an increase in packaging or die area costs. In addition, it is not enough to provide just one supply voltage level. Various components in a system-on-chip (SoC) can operate from different levels to optimize performance; or the core of the processor might require multiple voltage levels to reduce power or boost performance based on computational demand.

One possible approach to achieve discrete voltage levels is to switch each core individually to different supply rails provided by external regulators. While the approach might be beneficial for systems with very large number of cores, it significantly complicates the power supply routing [47], taking away entire metal levels normally available for signal routing. This complication limits the number of possible rails to two, at most three levels. Considering excessive supply pin overhead is significant for future scaling [18], additional power planes only compound the problem. In addition, care must be taken when switching cores from one supply to another by either scheduling power gating events [41] or reducing the supply plane impedance, using additional metal layers or finally, by increasing decoupling capacitance area [11]. Note this is all in addition to an increase in board component cost due to additional regula-

tors. As will be shown in this work, instead of adding static decoupling capacitance, using an on-chip switched capacitor converter can perform dynamic supply regulation while at the same time relax the impedance requirements placed on power supply routing by delivering power at a higher voltage.

## 1.2 Modern Dynamic Voltage Scaling

In addition to reduced system cost, one of the key benefits of on-chip regulation is the potential for fine-grain voltage scaling in both time and space and level. Dynamic voltage and frequency scaling (DVFS) is perhaps one of the most well studied techniques for adaptively balancing performance and energy efficiency. DVFS has been leveraged to improve energy efficiency at similar performance [6, 15, 23, 31, 47], operate at an energy-minimal or energy-optimized point [7, 12], improve performance at similar peak power [4, 10, 30, 32, 38, 39], and mitigate process variation [35]. Most of these studies assumed off-chip voltage regulation is best used for coarse-grain voltage scaling. In the past, this approach worked well since the CPU was the computation bottleneck; almost always busy, it required maximum supply voltage for relatively long periods of time. Over the past two decades, however, continuous improvements in process technology lead to a steady improvement in computing performance. This can be largely attributed to decreased device size, which lead to smaller interconnect and device capacitance, as well as lower on-resistance of transistors. Combined, these effects resulted in reduction of total RC delay enabling faster microprocessor clocks, while small device size enabled shift to parallel computation architectures on a single die. As a result, the CPU core often has to wait before it can start a new task as more data needs to be fetched from bandwidth

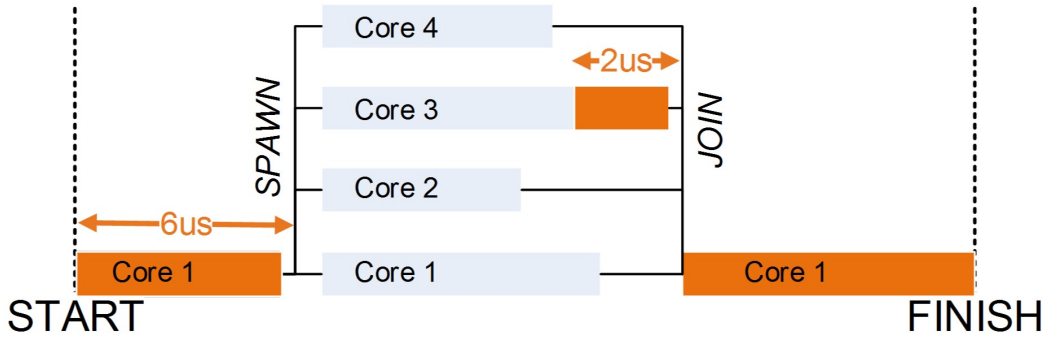


**Figure 1.1: Illustrative Multithreaded Application Activity Profile–** Variation in activity across cores produces opportunities for Fine-Grain Voltage Scaling for speedup during sequential code execution or energy saving for inactive cores. Light blue = active, parallel; orange = sequential code; white = waiting for work or join.

limited memory; or has to wait until other threads finish processing in case of multithreaded synchronization barriers

Traditional off-chip switching regulators operate at low switching frequencies due to the availability of large, high-Q passives and the desire to reduce switching losses due to parasitics. They also have longer control latencies due to slow switching speeds and parasitics between the on-chip load and the off-chip regulator, resulting in voltage scaling response times on the order of tens to hundreds of microseconds [5, 26, 27]. On-chip switching regulators can leverage faster control loops and are tightly integrated with the on-chip load enabling voltage scaling response times on the order of hundreds of nanoseconds. Figure 1.1 illustrates the potential for fine-grain voltage scaling in a modern, multi-core processor that would be out-of-reach for traditional off-chip regulators. Activity imbalance causes a core one to create a performance bottleneck according to the well know Amdahl's Law [2]. Increasing the voltage of active cores and decreasing the voltage of idle cores during this bottleneck could enable performance improvement within the same power envelope; but this is

only possible with per-core voltage scaling on the order of hundreds of nanoseconds [6,34,36].

### 1.2.1 Single-Threaded Workloads

When considering the requirements on the DC-DC voltage converter, it is imperative to understand the behavior of the load. In this case, we look at an in-order eight-core processor with private L1 instruction and data caches and a shared L2 cache. First we look at single-threaded execution across a number of benchmark applications. Such applications can only be executed on a single core and do not benefit from parallelization. In this case study, the other cores are waiting for work to be assigned. As such, their power requirements are very low and this leads to slack in the power budget across the whole chip which can be exploited to increase the voltage and frequency of the one core that is doing useful work. According to the DVFS plan described in more detail in Section 4.1.2, and cycle-level architecture simulator results, going from 0.8V supply to 1.1V supply results in 41-64% speed up in execution time depending on the benchmark. This speed up comes at the cost of various power overheads depending on organization of voltage domains detailed in Section 4. It is clear that DVFS can reduce execution time, but a careful consideration of the power delivery network and its trade-offs can lead to significant energy and area savings. Multi-threaded workloads analyzed in the next section require even more detailed analysis that also includes accurate voltage transition times.

### 1.2.2 Multi-Threaded Workloads

Multi-Programed workloads described in the previous section are one example of a loading scenario where benefits of fine-grain DVFS can improve performance of sequential code. A more challenging case is for parallelized workloads that are evenly distributed among the cores. At first it might seem that there is little that can be done to improve performance without directly increasing the power i.e. boosting the voltage of all the operating cores. However, a closer look at the sample applications kernels reveals workload imbalance, synchronization overheads and unparellelizable sections of code, which are all opportunities for speed up [4, 35]. The question remains if it is physically possible to exploit each application's particular behavior to improve performance by using the least amount of power (higher energy efficiecny). This relationship can be quantified by the 'isopower' line in Figure 1.2, which indicates a 1-to-1 correspondence between speedup and energy. Note that traditional DVFS usually results in 1-to-2 relation due to the well known dynamic power's quadratic dependence on supply voltage. In Figure 1.2 the impact of the converter properties is explored on a set of representative multi-threaded applications running on eight cores. In order to decouple the three variables of interest, namely the number of voltage levels (a), number voltage domains (b) and converter's response time (c), each is swept while keeping the remaining variables at the best possible value. These results effectively place design requirements for the converter. For example, blue stars represent configurations where energy is saved, but no performance improvement is obtained. Conversely, maroon triangles, result in dramatic reduction of execution time with a marginal improvement in power. In general, applications that benefit most from fine grained DVFS move towards the top right part of the plot. Example of such applications are shown

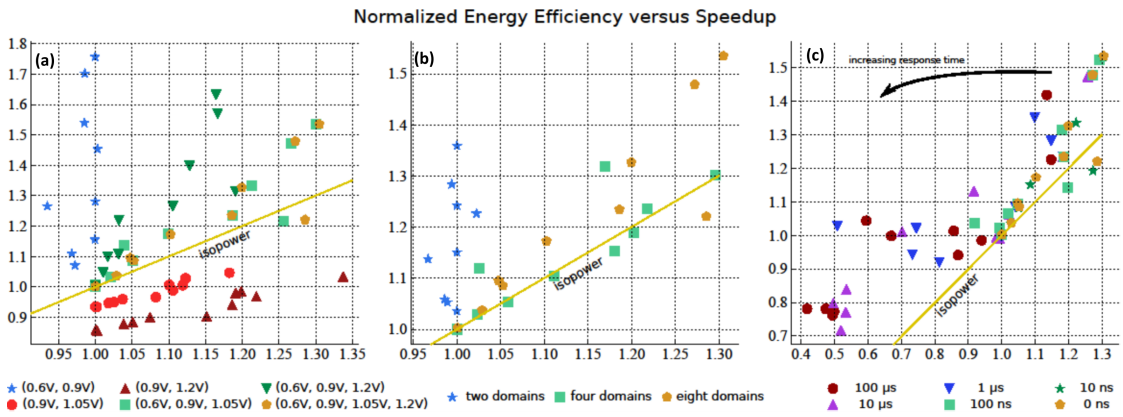


**Figure 1.2: Fine Grain Voltage Scaling Exploration in Level, Space, and Time** – Normalized energy efficiency (Y-axis) vs speedup over a baseline system with no DVFS. Points are applications simulated with the given controller. (a) controllers with different combinations of voltage levels. (b) 4- voltage level controller with different numbers of voltage domains. (c) 8-domain, 4-voltage-level system while sweeping response time per 0.15 V step. **Courtesy Christopher Torng*

in Figure 1.3, where a real-time control algorithm assigns voltage level based on core activity. Breadth-First-Search benefits most from multiple voltage levels, LU factorization from multiple voltage domains, and Radix sort has many short synchronization barriers that require fast transition times.

## 1.3 Problem Statement

Architecture results from Sections 4.4 and 1.2.2 show that there is significant opportunity to improve performance in modern multicore processors if the voltage converter is efficient across a wide range of output voltage and current levels, small enough to supply each core individually, and can provide very fast voltage transitions. Traditional off-chip switching regulators are inadequate because they are expensive, bulky, and obviously require dedicated power pins and on-chip power distribution networks, limiting the number of independent on-chip power domains; on-chip switching regulators can be located close to

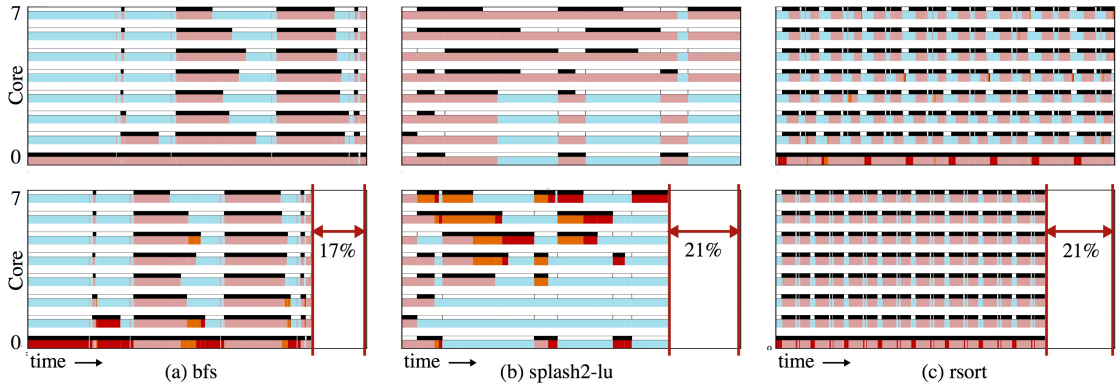


**Figure 1.3: Application Activity Plots –** Rows show DVFS controller decisions per-core (0.6V = blue, 0.9V = pink, 1.05V = orange, 1.2V = deep red). Horizontal strips above cores show actual activity (active = black, waiting = white). Illustrates impact of Fine Grain Voltage Scaling parameters on speedup: (a) in voltage level on breadth-first search with 2 (top), 4 levels (bottom); (b) in space on SPLASH-2 LU factorization with 2 (top), 8 domains (bottom); (c) in time on radix sort with 1 us (top) 100 ns (bottom) response time. **Courtesy Christopher Torng*

each core enabling per-core voltage scaling with fine grain time intervals. However, satisfying all these requirements simultaneously is difficult if not impossible for on-chip regulators. So the real system design challenge is to provide fine-grain voltage scaling in time, space, and level with minimal area and efficiency overhead.

## 1.4 Collaborators, Publications, Funding

Part of this work would not be possible if it were not for inspiration and collaboration with Dr. Christopher Batten and Christopher Torng from Computer Systems Laboratory. Dr. Batten's key insights into multicore chip-wide power cap, together with the author's analysis of switched capacitor circuits and Dr. Apsel's observations on switched capacitor area and power handling capability, lead to the formulation of RPDN as a concept. In addition, Dr Batten's input on

paper submissions to ISCA and MICRO conferences, such as conceptualization of the power distribution networks for switched capacitor converters, was invaluable. The architecture results were obtained by Christopher Torng, who has done tremendous work bringing up test applications and gem5 simulator with good energy models based on RTL, as well as the DVFS controller. Christopher Torng also contributed to the design of the RPDN test chip with layout of the custom SPI interface chain. I would also like to thank Ivan Bukreyev who took over the responsibility for design and layout of the VCO and the charge pump, as well as adapting a previous comparator design for the RPDN test chip. Ivan also layed out a very compact and challenging part of the cluster level. The author would also like to thank Hahn-Phuc Le from Berkeley for his suggestions on using the one-shot block.

For the 3-level converter design, Bo Sun helped with part of the layout and delay blocks. The testing of the chip would not be possible without the help of Carlos Dorta, who did most of the painstaking bondwiring, and Tanay Gosavi who diced the chips so that they could fit in the package. The test system was based on FPGA code and DAC boards developed by Dr. Xiao Wang. The asynchronous state machine in the 3-level buck converter was a modified version of one initially thought out by Dr. Paula Petrica.

The author would also like to thank the TSMC shuttle program for enabling the fabrication of the 3-level converter and also the graduate fellowships from I. Jacobs and C. Sporck as well as Department Of Energy grant.

# Chapter 2

# Approaches to Fully Integrated Voltage Regulation

The three primary types of step-down voltage regulators are linear regulators, inductor-based switching regulators known as Buck converters, and capacitor-based switching regulators. These regulators can be evaluated based on four key metrics: (1) *integration complexity*, i.e., does the regulator require extra non-standard fabrication steps?; (2) *area overhead and power density*, i.e., how much regulator area is required to deliver a certain amount of power?; (3) *power efficiency*, i.e., ratio of the output power to the supplied input power; and (4) *response time*, i.e., how fast can the target output voltage be adjusted?

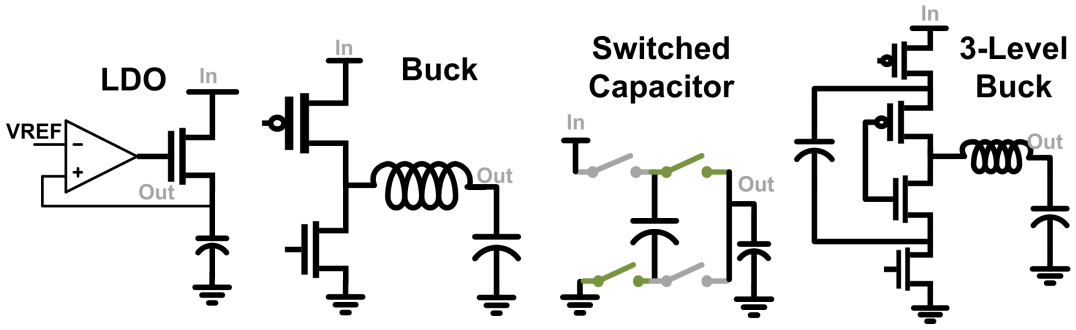


**Figure 2.1: Four Step-down DC-DC converter types** – ordered from the simplest (LDO) to most complicated (3-Level)

## 2.1 Low-Dropout Regulator

*Linear voltage regulators* (also called low-dropout (LDO) regulators) are an example of a non-switching regulator. LDOs use a power MOSFET as a variable resistor, with a high-gain amplifier wrapped in a feedback configuration to reduce output resistance as shown in Figure 2.1. The feedback loop holds the output voltage at a predetermined value while adjusting the gate voltage of the FET to support the load current. At first glance, the lack of energy storage elements seems to imply LDOs will have much lower area overheads. However, a large decoupling capacitor is still required, as the feedback loop in the LDO has limited bandwidth. Thus, 10–15% of the chip area must still be reserved for decoupling capacitance to maintain supply integrity and to prevent voltage emergencies in adjacent cores or logic during large current steps [16]. In addition, the maximum efficiency that can be achieved is the ratio of the output/input voltages since the MOSFET and amplifier effectively act as an adjustable resistance. This means that linear voltage regulators are highly inefficient for large voltage drops. For example, if the off-chip voltage level is 1.8 V and the target on-chip voltage level is 0.8 V over half of the power consumed by the chip will be wasted as heat in the linear regulator.

## 2.2 Buck Converter

*Inductor-based switching voltage regulators* (also called Buck converters) are the traditional off-chip regulator of choice due to the potential for good efficiency over a wide voltage and current range as well as excellent voltage regulation capabilities. Buck converters store energy in an inductor (Figure 2.1) which

switches from a series configuration with the high voltage supply (the energy storing configuration) to a parallel configuration where the supply terminal is switched to ground (the energy from the inductor dissipates to the load in this configuration). If the inductor is small, the energy is dissipated quickly in the load requiring faster switching. In a fully integrated, on-chip buck converter, the efficiency is severely limited by the size and parasitics of the inductor and, to a lesser extent by the power switches. Reduction of integrated inductors' parasitics is the key to an efficient buck converter as shown in recently published work in this area [1, 17, 22, 26]. These designs have reasonable efficiencies, but only for relatively low step-down ratios which make them less suitable for the wide dynamic range required for fine-grain voltage scaling. While the efficiencies of recent designs are acceptable, the inductors used in these regulators provide relatively low power densities on the order of $0.2\,\mathrm{W/mm^2}$. Unfortunately, solutions with higher power densities require magnetic materials, complicated post fabrication steps, or interposer chips [45, 53].

## 2.3 Switched Capacitor Converter

*Capacitor-based switching voltage regulators* (also called switched-capacitor (SC) regulators) work by alternately switching a set of capacitors with a given divide ratio from series (charge up) to shunt configuration (discharge) fast enough to maintain the voltage across a load (Figure 2.1). SC regulators are capable of excellent efficiencies, but can only support certain discrete voltage divide ratios (e.g., 1/2, 1/3, 2/3) and must incorporate more than ten phases to reduce ripple losses [43]. Pulse Width Modulation is not as effective in controlling the output impedance of the converter and thus regulating the output voltage. Duty cycle change from 10% to 50% only changes the output impedance of the converter

by about a factor of 5 [24] with a decrease in efficiency. Instead, frequency modulation is typically employed to regulate the output. The regulation and output voltage range shortcomings of SC converters are balanced by the potential for higher power densities of 0.8–2 $W/mm^2$ [8,29,44] when using energy-dense on-chip capacitors. Note that in contrast to Buck converters, the energy density of MOS, MIM, and deep trench capacitors is sufficient to avoid the need for any off-chip or in-package energy storage elements. Due to the nature of operation, half the capacitance in a SC regulator is always seen between the regulator output and ground and is acting as effective decoupling capacitance [29]. This means that an explicit decoupling cap may not be necessary, which can further reduce the area overhead of SC regulators. Unlike buck converters, which are fundamentally impossible to reduce for smaller loads without incurring prohibitive losses, SC regulators can be easily scaled by simply adjusting the size of the capacitor and the switches. The reader is refered to survey works [42,44,51] for further discussion about these topologies.

## 2.4 Hybrid / Multilevel Converter

A Hybrid converter is a combination of of Buck and SC converters. The first order benefits of such configuration can be understood by an explanation given by M. Seeman [43] who considered a SC converter presented with an inductive load. This is somewhat unusual, as most loads on chip are capacitative with some small resistance in parallel resulting in an efficiency profile as discussed in previous section. Nevertheless, a large inductive load can lead to 100% efficiency across a range of output voltages. This property has been exploited in [37], where a switched capacitor converter is followed by a buck regulator. One of the biggest advantages of SC converters is the voltage blocking prop-

erty, i.e. the flyback capacitor acts as an effective high voltage shield for the switches. Crucially, none of the switches experience a full supply voltage swing across its gate-source/drain terminals. As a result, better performing switches with lower breakdown can be employed, which significantly reduce switching and resistive losses. While it is possible to use stacked devices to operate a buck converter with higher supply than the rating of the switches [5], it is a significant design challenge. It is perhaps no surprise that first implementations of hybrid converters were for high voltage applications [27] and [55]. More recently, the multilevel converter was revisited for integrated or semi-integrated solutions [14] as they can typically employ a smaller inductance compared to a pure buck converter. The relative advantages compared to buck have been throughly investigated in [49] [22]. Operation of a 3-level converted is described in detail in Section 3. Similar to a SC converter a flyback capacitor is charged in series with the load and discharged in parallel with the load through an inductor. Additional states involve bypassing the flyback capacitor and connecting the inductor to either ground or supply as in a buck converter. It is those two additional states that allow a hybrid converter output to be sensitive to PWM control. In case of a pure SC converter pulse width has limited effect on the output as mentioned in previous section.

## 2.5 Case Study - Stepping Down a 3.3V Supply

To understand the impact of the converter on system power, it would be instructive to study a particular case of voltage conversion. Suppose our goal is to provide power to four independent loads from a Lithium-Ion battery, whose voltage can range from 2.9-3.7V. We would also like to adjust the voltage at each load with the following levels: 1.2, 1, 0.8 and 0.6V. An off-chip converter steps

down from 3.3V to either 1.8V for an on-chip SC converter or to 1.4V for on-chip LDO as illustrated Figure 2.2. We chose 1.8V as input, which can be easily implemented using structures presented in this work later on, but most recent works in SC integrated converters are using more complicated topologies with the goal of directly converting battery to load level, obviating the need for an external regulator. In [28], the authors achieve 73% efficiency with 5:2 ratio in 65nm CMOS albeit with reduced power density of $0.19W/mm^2$. Trench capacitors hold great promise for increasing the power density significantly, but for now their availability is still limited.

The total power drawn from the battery in Figure 2.3 is plotted vs. the system efficiency. System efficiency reflects the amount of power that is actually delivered to the load. The combined efficiency of the two voltage converters in series is simply a product of their respective efficiencies. In our study, as the load voltage is reduced, the power at the load also decreases according to a DVFS plan detailed in Section 4.1.2. Efficiencies at higher load power/voltage are relatively more important, but it also depends on the amount of time the load operates at each voltage. Using four external converters is the most efficient solution, but costly for reasons described in Section 1.1. Instead, if we use an external converter to supply the on-chip LDO, most of the power from the battery is dissipated in the LDO as opposed to the load. This results in abysmal system efficiency at low voltages. On-chip switched capacitors come somewhere in between those two in terms of the system efficiency, allow for fast changes in voltage, which the external converters are not capable of. In addition, the voltage presented to the chip is 1.8V which would likely be required anyways for I/O and other peripheral circuitry. A brief survey of on-chip efficiencies reported in literature is presented in Figure 2.4 and compared against

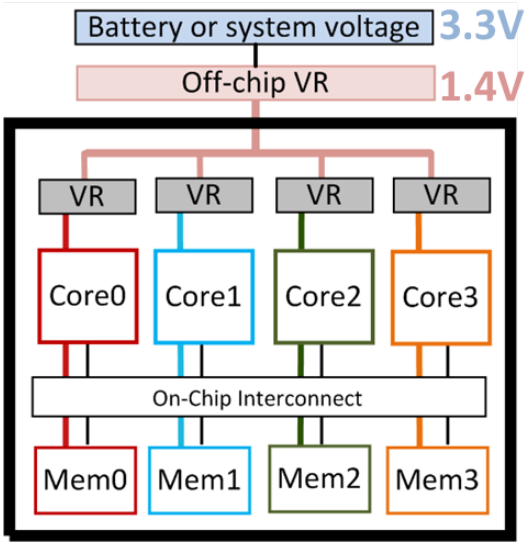


**Figure 2.2: Diagram of a Case Study –** Battery voltage is a 3.3V, which is stepped down to 1.4V for LDO operation and 1.8V for Switched Capacitor.

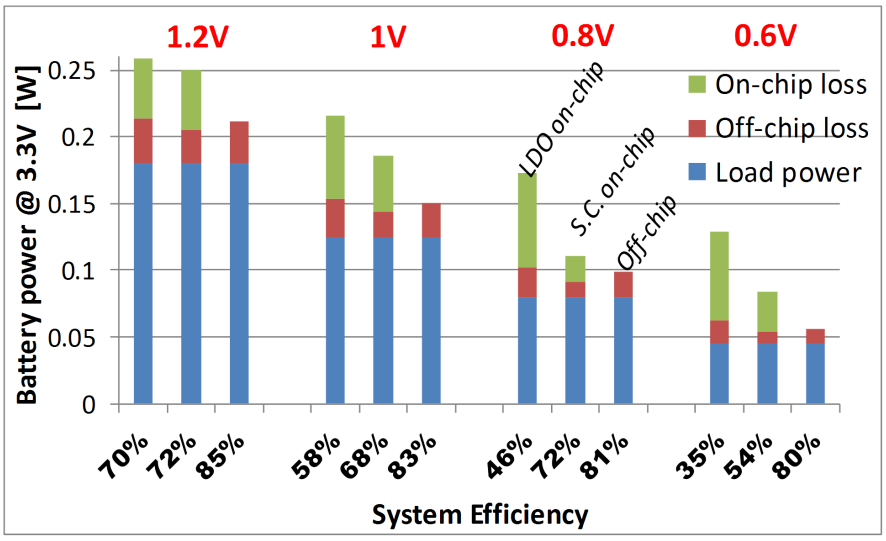


**Figure 2.3: System Power Distribution for Voltage Regulators and Load –** LDO is very inefficient especially for wide DVFS voltage range. Four external regulators are most efficient but most expensive.

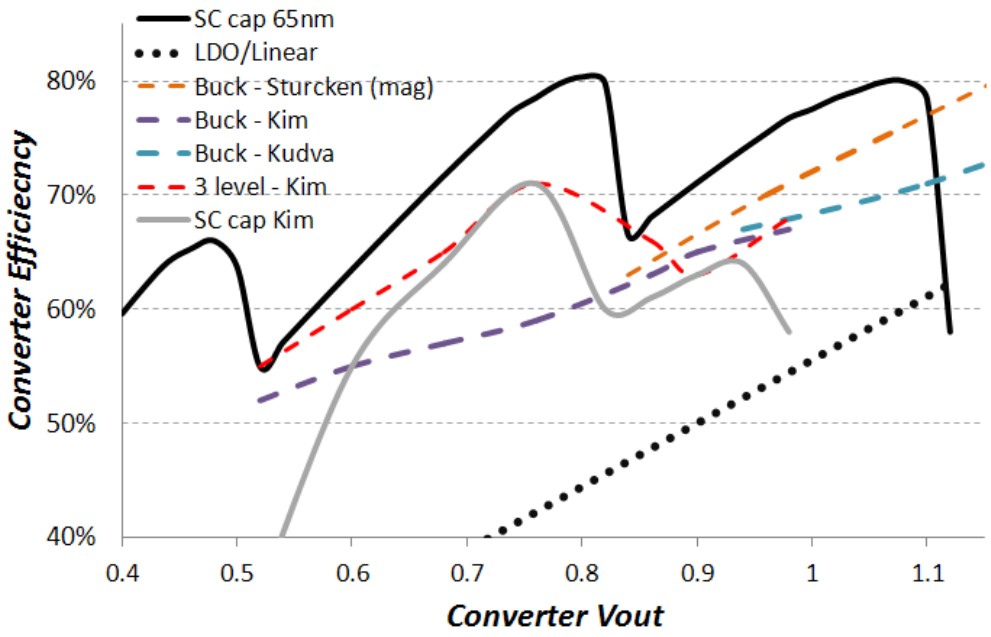


**Figure 2.4: On-chip DC-DC Converter Efficiency Estimate** for three types of regulators for 1.8V input vs. output voltage based on published results Kudva [26] and Kim [22] (130nm), Sturcken [45] (45nm) normalized for the voltage conversion ratio. SC converter is based on a 65nm analytical model prediction [43].

a best case LDO efficiency. However, directly comparing efficiencies of designs targeting different voltage and current ranges in various technologies is incorrect. To estimate the potential performance of various converters types a normalization is performed for the same conversion ratio as follows. $\eta_{norm}$ (the normalized efficiency) is equated to $\eta$, the efficiency reported in publication, when $Vout_{norm}/1.8 = Vout/Vin$. This is possible when the reported voltage conversion in a particular design overlaps our target conversion ratio for 1.8V input. Note that this comparison disregards current range capabilities of the converter, so this is just a first order estimate. Interestingly, buck designs in [22,26] track very closely and design in [45] uses magnetic materials in inductors and has a visible improvement. In addition, there is a clear improvement for SC converters with improving process technology as both switches and capacitor density im-

prove. While on-chip switching supplies achieve higher efficiencies than LDOs, they come at significant die area overhead and minimizing this overhead is one of the key challenges in on-chip power conversion. Ultimately, the best solution will vary from system to system and will likely involve a combination of these approaches for most complicated systems, depending if the design priority is die area, board area, low power, performance and component cost. As performance (efficiency and area) of on-chip switching converters improves, the balance will tip in favor of more integration.

# Chapter 3

# Design of a 3-level Buck Converter for Coarse Grain Voltage Domains

While there has been progress in the integration of on-chip buck converters, these designs are limited to low step-down (high conversion) ratios as seen in Figure 2.4 and therefore have difficulty achieving high efficiency for low-power processor sleep states [26, 52]. These states can account for as much as 98% of the operating time of a processor in low-power wireless sensor applications [25]. Alternatively, integrated switched capacitor converters achieve up to 80% efficiency for high voltage step down ratios, but only for a narrow output voltage range [19,29]. 3-level converters combine the advantages of both topologies [22] for large output currents in continuous conduction mode (CCM), but like integrated buck converters, perform poorly for low currents and voltages (Figure 3.1) due to lack of large on-chip inductance. In this work, we present a design that provides similar peak power performance per area as [22] by using up to two interleaved phases and PWM control and adds important low current and voltage output capability to regulate processors operating in low power sleep or resting states. Our key insight is that the unique 3-level converter topology

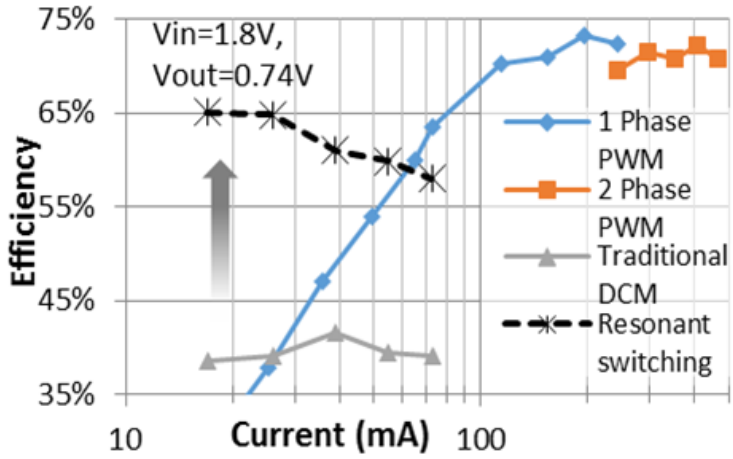


**Figure 3.1:** Simulated efficiency across load currents for 3-level converter in continuous conduction mode, using DCM at low currents, and with proposed resonant switching at low currents.

allows for the use of a resonant soft switching state in place of a traditional discontinuous conduction mode (DCM). This resonance is unique to this topology and is not a characteristic of either buck or switched capacitor converters, but allows for a dramatic reduction in switching losses. We achieve up to 64% efficiency at high conversion ratios and low powers by using this part-time resonant switching mode in place of traditional DCM. To accomplish this, a low latency asynchronous state machine controls each power switch independently. The operating mode is selected by dynamically detecting peak current through the inductor and the voltage across the flyback capacitor (CFLY) (Figure 3.5) rather than relying on fixed timing schemes [49, 52]. This results in dramatic improvements of 60-80% in efficiency over DCM mode as shown in Figure 3.1.

## 3.1 Traditional Switching Strategies and Operation

The switching strategies in a 3-level converter can be adapted from a traditional buck topology with a some modifications. It is instructive to consider them in

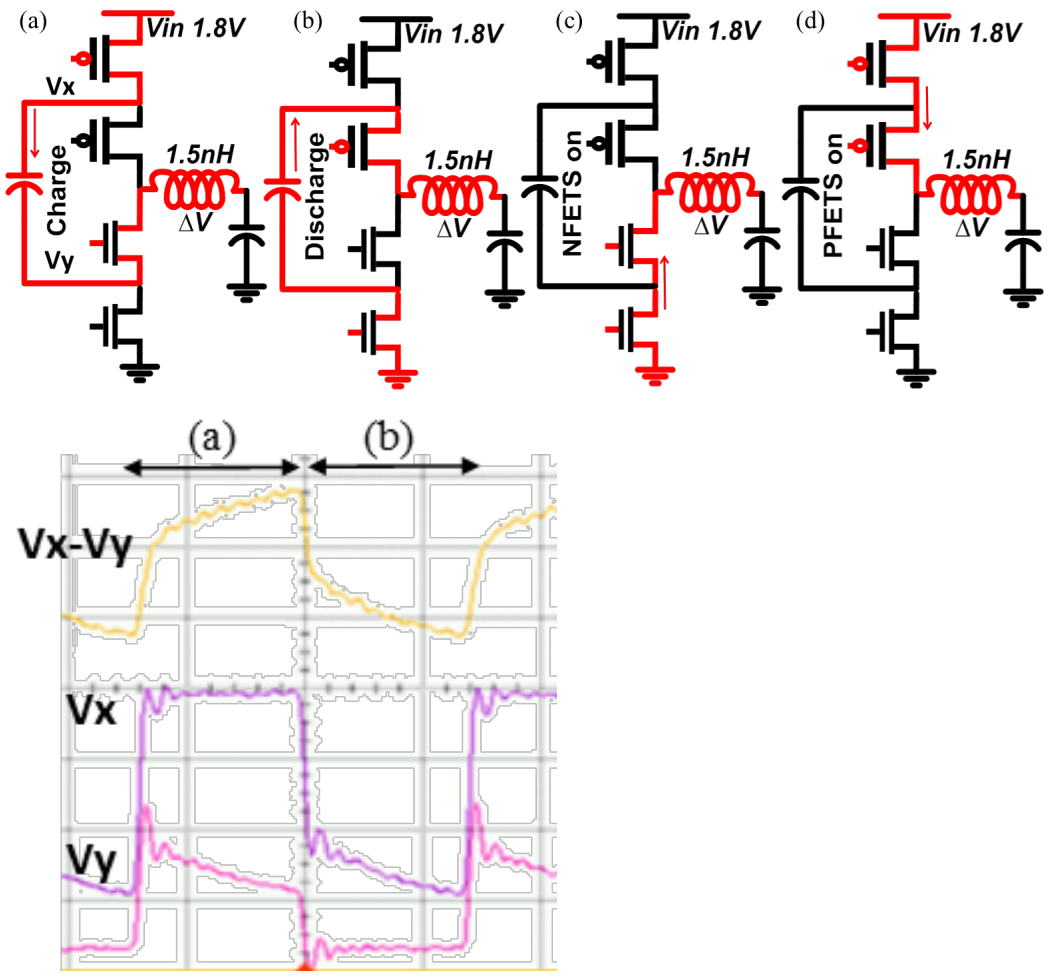


**Figure 3.2:** 3-level converter current path in red for (a) charge mode configuration, (b) discharge mode, with the measured waveforms on nodes Vx and Vy, (c) path for releasing energy stored in the inductor in CLC cycle, (d) bypassing CFLY in DCM mode. Also shown are the measured voltage waveforms at nodes Vx and Vy during cycles (a) and (b) and their difference.

more detail to understand the benefits and limitations of a 3-level converter. In this section we describe the *continuous conduction mode* – CCM, which achieves very good efficiency compared to a similar buck design at high currents. This is what makes the 3-level converter such a promising topology. Conversely, the *discontinuous conduction mode* – DCM for low currents is especially troublesome for fully integrated inductive converters with very small inductors.

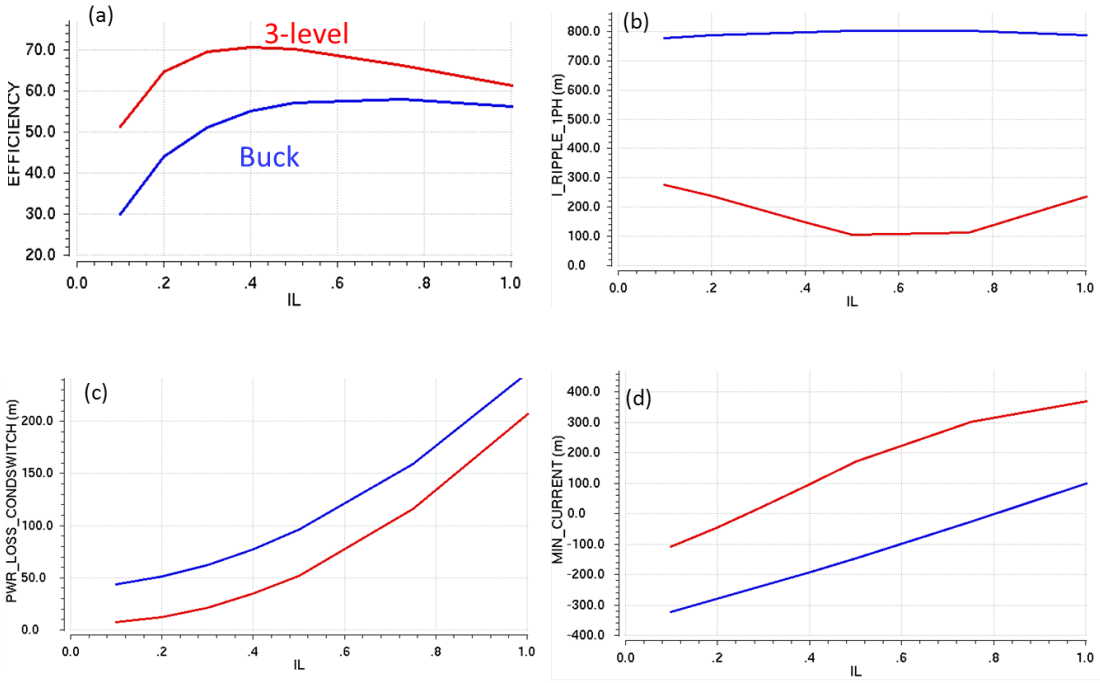


**Figure 3.3:** (a) Simulated efficiency of a 2 phase 3 level design compared against a standard buck for the same application using 65nm 1V MOS transistor. Note that buck must also use stacked transistors to satisfy 2V input voltage breakdown requirements. (b) Current ripple that leads to (c) RMS conduction loss in the inductor and similarly through the switches. (d) Peak minimum current - current flows in the opposite direction to from load to ground when NMOS is on, which necessitates the onset of DCM mode.

### 3.1.1 CCM for High Currents

The basic topology of a 3-level converter is shown in Figure 3.2. 3-level converters reach peak efficiency when the output voltage is at half the input voltage for no load. In this mode the operation most closely resembles that of a switched capacitor converter; in that the circuit is switched to alternately charge the flyback capacitor in series (Figure 3.2a) and discharge it in parallel (Figure 3.2b) with the load while maintaining Vdd/2 across the flyback capacitor. In CCM, two additional modes of operation are used that bypass CFLY and directly connect the inductor either with ground or supply (Figure 3.2c,d) exactly as in a

standard buck converter. PWM can be applied to combine all these modes to regulate the output voltage as demonstrated in [22].

### 3.1.2 Comparison to Buck

Previous work explored the relative differences between a buck and a 3-level converter [22, 50, 54]. Generally, the comparison is not straightforward, especially for fully integrated converters. Factors such as inductor and capacitor area, output ripple, voltage blocking capability, conversion ratio, and load current range have to be carefully renormalized for each design for a fair comparison. However, to better understand why a 3-level design is advantageous, 1st-order designs of a buck and 3-level converter have been compared through simulations in CCM mode. The results in Figure 3.3 show that the 3-level has better efficiency brought about by reducing the current ripple (and thus the RMS current power loss). This reduction is only advantageous at input/output voltage divide ratios close to 2, which explains the results in Figure 2.1. Note that multi-phasing in a buck converter doesn't improve the current ripple through each inductor, only the output voltage ripple.

### 3.1.3 DCM for Low Currents

As the load current decreases, the switching frequency of the converter must also drop, decreasing switching, conduction, and gate drive losses relative to low output power. Thus both buck and 3-level converter show a sharp drop in efficiency below 200mA in Figure 3.3. In addition, the decrease in switching frequency causes a large output ripple as indicated by measurements in Figure 3.12. In switched capacitor converters, 10 or more phases are interleaved to alle-

viate this [29]. However, there are significant area and design penalties to using many phases in 3-level or buck type circuits. Using additional phases (each of which is provisioned for high power operation) requires that each phase deliver less current for a given load. This drops the switching frequency for each phase, further exacerbating the problem. The result, as can be seen by the CCM curves in Figure 3.1, is a dramatic drop in efficiency at low currents. The traditional solution to this is to employ discontinuous conduction mode (DCM) for light load conditions. In light load conditions, the inductor current builds quickly and must be discharged by fast switching of the NFETs (Figure 3.2c). The capacitor is also bypassed in charge mode by turning on the PFETs (Figure 3.2d) to prevent overcharge of the capacitor, resulting in the same DCM configuration that would be used in a traditional buck converter. This approach leads to poor efficiency for integrated 3-level converters (Figure 3.1), with small inductors. High frequency switching required to limit ripple in this mode leads to additional gate drive loss; while large voltage drops across the switches increase conduction losses (Equation 3.1) and switching loss (Equation 3.2).

$$P_{cond} = R_{nmos} I_{nmos}^2 = \sqrt{\frac{8 I_o^2 V_o (V_{in} - V_o)^2}{9 L V_{in}^2 f_s}} \tag{3.1}$$

$$P_{sw-nmos} = \frac{1}{6} f_s T_{sw} V_{in} \sqrt{\frac{2 I_o V_o (V_{in} - V_o)^2}{L V_{in} f_s}} \tag{3.2}$$

Here, $V_o$ and $V_{in}$ are output and input voltages, $f_s$ is the switching frequency, $I_o$ is the load current, and $T_{sw}$ is the time it takes to turn a switch on or off and depends on driver strength. Similar expressions can be found for the PMOS. There is also additional conduction loss due to the inductor.

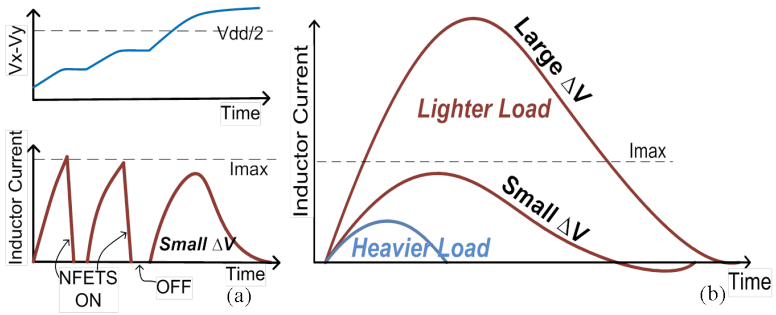


**Figure 3.4:** (a) Flyback capacitor voltage and inductor current waveforms with part time resonant switching, onset of current limiting depends on load (b) Inductor current over time in typical 3level converter.

## 3.2 Part-Time Resonant Switching

As noted in Equations 3.1 and 3.2, the primary loss mechanisms in DCM are the conduction loss and the switching loss. For a given inductor size, the conduction loss is inversely proportional to the switching frequency while the switching loss and gate drive loss are directly proportional to the switching frequency. In order to reduce these losses, we introduce a novel technique that utilizes the series combination of the flyback capacitor and inductor to perform efficient soft switching at low current loads. We observe that the combination of the flyback capacitor and series inductor can produce a resonance that allows for soft switching of the inductor. For small voltage drops across the inductor, this resonant effect can avoid hard switching and the associated losses altogether. However, this effect must be controlled for large $\Delta V$ to prevent very high peak currents and ripple shown in Figure 3.4b. The proposed part-time resonant switching scheme has two regimes of operation, the current limit cycle (CLC) and the quasi-resonant mode (QRM). During the CLC, peak currents are limited by switching, while in QRM, the circuit leverages its natural transient response for higher efficiency. Assuming the same size and quality of inductor,

the mechanisms for loss during the CLC and the QRM are different from those of typical DCM operation. During a CLC, there is conduction loss and switching loss which take a form similar to the losses shown for DCM in Equations 3.1 and 3.2. In CLC, these losses are reduced in two ways. First $V_{in}$ in Equation 3.1 is replaced with $V_{in}/2$, because we use the charge and discharge configurations from CCM shown in Figure 3.2(a) and 3.2(b) resulting in a smaller voltage presented to the inductor. Second, the switching frequency $f_{sCLC}$ is much lower than $f_{sDCM}$. This is because the slope of the inductor current is much greater in DCM (Equation 3) where the flyback capacitor is bypassed vs in CLC (Equation 4) [50].

$$I_{L,DCM} = \frac{V_{in} - V_o}{L} t_{onDCM} \tag{3.3}$$

$$I_{L,CLC} = (\frac{V_{in}}{2} + \frac{I_o V_o}{2 C_{FLY} f_{sCLC} V_{in}} - V_o) \sqrt{\frac{C_{FLY}}{L}} \sin \frac{t_{onCLC}}{\sqrt{L C_{FLY}}} \tag{3.4}$$

Thus, the inductor reaches the same maximum current much faster in DCM than in CLC mode and the PMOS on time $t_{ON,DCM}$ is much smaller than $t_{ON,CLC}$. This necessitates a much faster switching frequency in the case of DCM, and higher switching losses as seen in Equation 3.2 by a factor of about three. In QRM there are no hard switching events, i.e., the switches are turned on/off when the current is close to zero. So the loss is dominated by intrinsic capacitor charge and discharge loss [29] and conduction losses only, eliminating the effects of Equation 3.2 altogether.

$$P_{cond} = \sqrt{(\frac{I_o^2}{4 C_{FLY} f_{sQRM}})^2 + ((I_o + \frac{I_{maxCLC}}{\sqrt{2}})^2 R_{tot}} \tag{3.5}$$

$f_{sQRM}$ is typically a factor of four smaller then $f_{sCLC}$ and $R_{tot}$ is total series resistance of the switches and inductor for a given charge/discharge path. A

comparison of Equations 3.1 and 3.2 and 3.3 to 3.4 and 3.5 indicates that elimination of hard switching events, and addition of a combination of resonance and ripple control can improve the efficiency for low current loads up to 62% for typical on-chip conditions. Figure 3.1 shows the simulated efficiency for a 3-level converter in traditional CCM and DCM modes as well as in part-time resonant switching mode. This simulation was performed using Spectre with the TSMC 65nm design kit using the PDK inductor with widest possible trace and shows the dramatic improvement across low current loads up to 60mA that result from this technique.

## 3.3 Circuit Implementation

In order to realize these benefits, we have designed a 3-level converter with part time resonant switching as shown in Figure 3.5 . In typical operation, CFLY is alternately charged (Figure 3.2a) and discharged (Figure 3.2b) through the inductor while maintaining Vdd/2 across the capacitor. The inductor current is small if $\Delta V$ across the inductor is small or the load demands high current (Figure 3.4b). However, as the load current decreases, the switching frequency decreases to regulate the output voltage. This causes a large output ripple and high peak current through the inductor. When a peak inductor current above a limit threshold is detected, the regulator goes into a CLC where both of the NFETs are briefly turned on to dissipate energy from the inductor to the load (Figure 3.2c). This limits output voltage ripple. A current limited cycle (CLC) is followed by an OFF state (where none of the transistors are conducting) (Figure 3.4a). To allow the OFF state, we modify the original circuit to allow P1 and N1 as shown in Figure 3.5, to be independently driven. After a few nanoseconds, the circuit senses the voltage across CFLY and the state machine determines

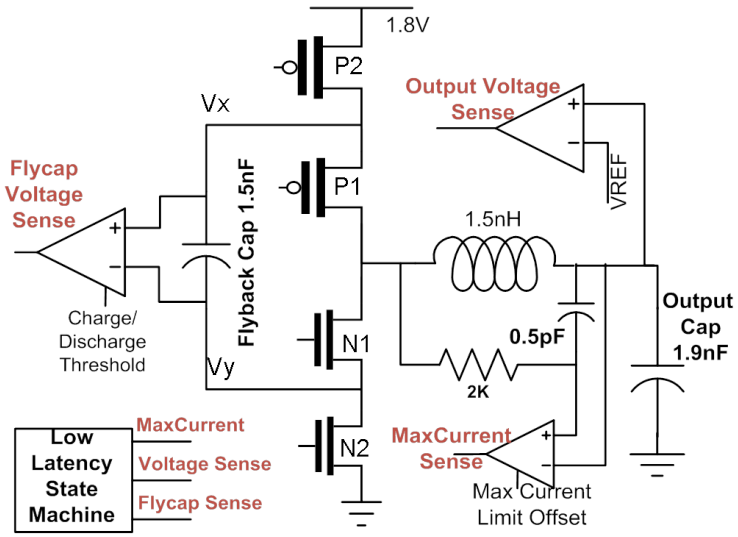


**Figure 3.5:** Simplified block diagram of proposed approach with observables.

whether to go into charge or discharge mode (Figure 3.2a and 3.2b), since the voltage across CFLY needs to be maintained at Vdd/2 for proper operation.

### 3.3.1 Observables and Event Detection

The determination of current mode is done by sensing the current through the inductor in real time. If the peak current sensed through the Max Current Sense circuit is above Imax, the circuit goes into CLC mode, limiting the current below Imax by switching on N1and N2 and by using the OFF state. If the inductor current doesnt cross this threshold, the circuit operates in QRM by staying in the same configuration and allowing the circuit to relax naturally as shown in Figure 3.4b. This combination of states allows limitation of ripple while minimizing switching losses.The Max Current Sense comparator has an adjustable offset so that Imax (and thus ripple or the number of CLCs) can be adjusted as desired. The RC network across the inductor acts as a high-pass filter with respect to inductor current, such that the steeper the inductor current, the more sensitive

the detection becomes. After a peak current is detected, a low-latency, asynchronous state machine transitions to the next switch state, whcih is to briefly turn on both of the NFETs and then go to OFF state as described above is done. The state machine diagram is shown in Figure 3.6. Minimizing the state machine and detection latency is critical, as together with buffer chain delay, it limits the lowest ripple that can be achieved. Since the buffer delay is fixed, and the logic delay is already low, to reduce the ripple further either an increase in L or C would be required. A more detailed circuit diagram is shown in Figure 3.10, which shows some of challenges associated managing multiple voltage levels used to drive the power fets.

### 3.3.2 Level Shifting and Power Drive Strategy

After an event is detected and processed by the state machine, the next switch configuration is sent to the decoder. This complete path can be seen in Figure 3.10. The full-custom decoder then translates each state bit description into the actual voltage levels to be applied to the mid-driver (Figure 3.9), level shifters (Figure 3.7) and tapered buffers. It is imperative to minimize the the delay through the whole chain to prevent undesirable interaction with the state machine algorithm. To this end, a capacitative level shifter is designed as it is much faster than a regenerative based latch. Previous implementations of capacitative level shifters include a resistor in feedback in the second, high voltage stage [29]. This solution biases the second stage around the inverter trip point, but imposes a lower frequency limit on the operation of the level shifter. The frequency limit is formed by the high pass filter composed of the resistor and capacitor combination. Since the 3-level converter in DCM mode can have extended non-switching periods that are difficult to predict, the resistive feed-

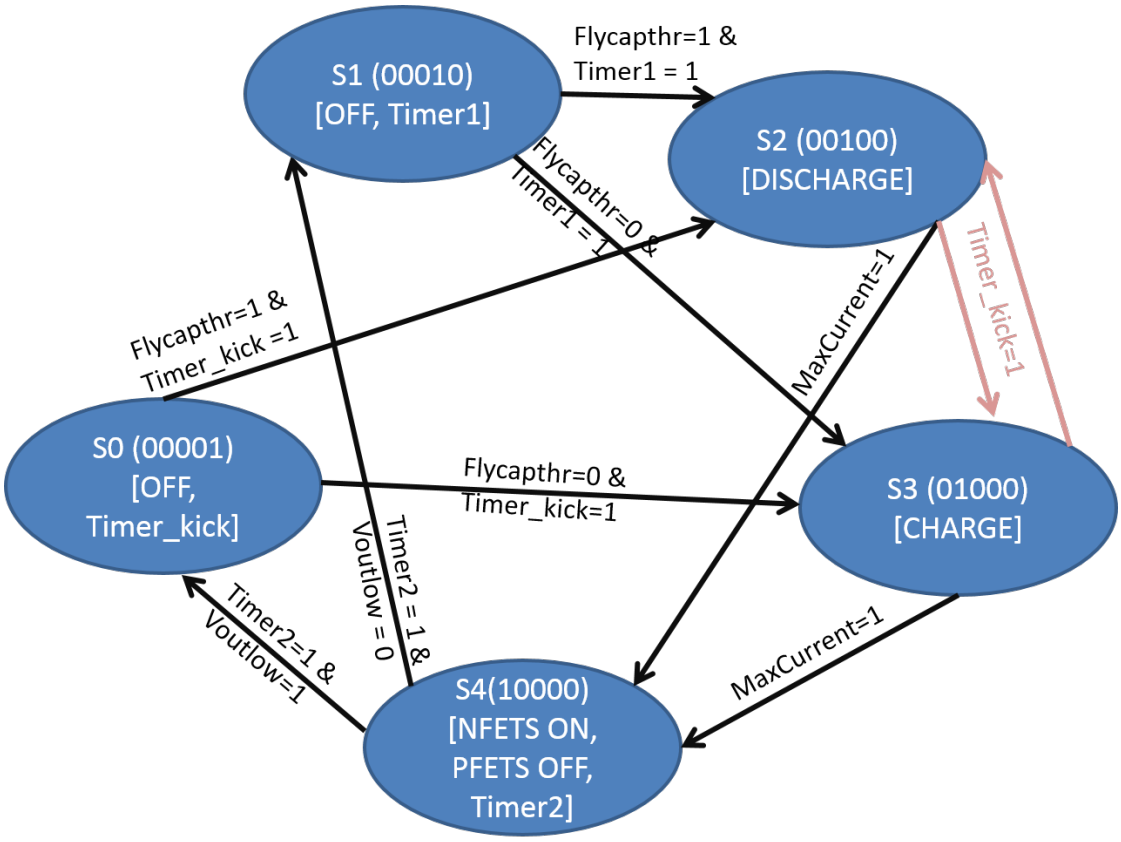


**Figure 3.6: One Hot, Asynchronous State Machine –** Simplified state diagram of the custom, ultra low latency state machine used to determine the next switch configuration. The critical aspect of the design is to minimize the latency to less than 150ps immediately after event detection. The arrows represent logic levels of event comparators or delay block outputs. Such low latency would not be possible with a clocked design in this process. One Hot design methodology forbids self-referenced states. Red arrows show departure from that methodology with custom logic.

back design is inadequate. Instead an inverter-latch based level shifter is used as shown in Figure 3.7. The latch operates between the 1V to 2V voltage levels. The inverter latch holds the state indefinitely, but one problem with this circuit that the initial state of the latch is undefined and possibly incorrect before the first transition occurs. To solve this problem two feedforward, high voltage (thick-oxide) transistors are employed. This feedforward path is slow, in the order of microseconds, but when the circuit is powered up, the supply increases

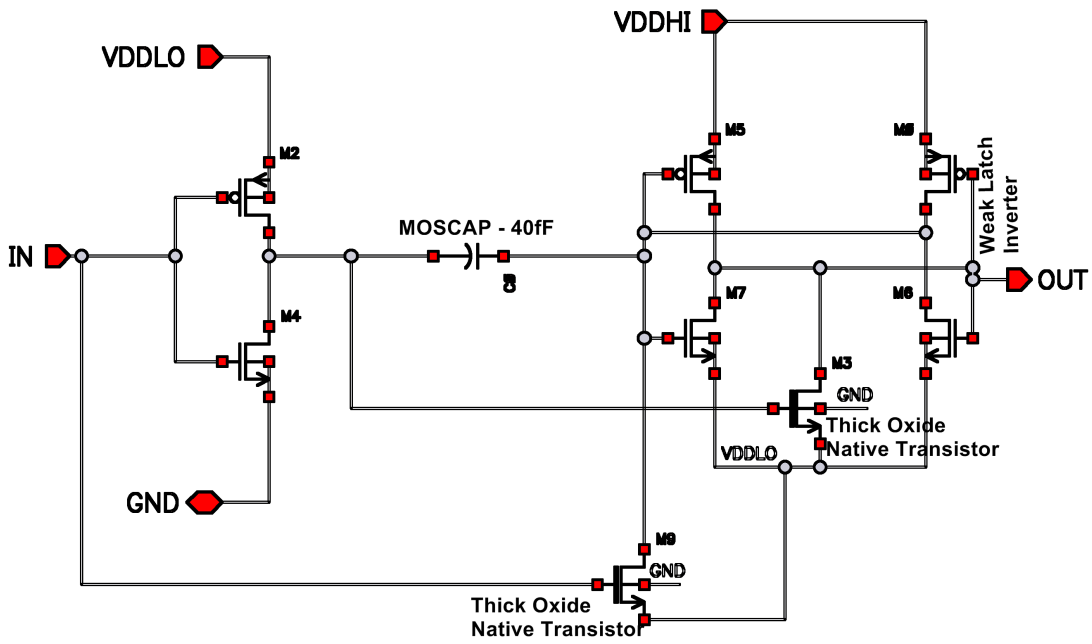


**Figure 3.7: 1-0V to 2-1V Capacitative Level Shifter –** is much faster then a regenerative latch design in Figure 3.8 as it only uses thin oxide devices, but only works above a certain frequency. Feedforward path uses native thick oxide transistors to ensure the correct state during startup. Latency is around 80ps.

on the order of miliseconds due to large decoupling capacitors present on the board or elsewhere.

### 3.3.3 Measured Results

We designed and fabricated a fully integrated 3-level buck converter using our novel part-time resonant switching technique in a TSMC 65nm process (Figures 3.16). For fair comparison across inductor size and process, we also implemented a traditional DCM mode as used in buck converters. The design

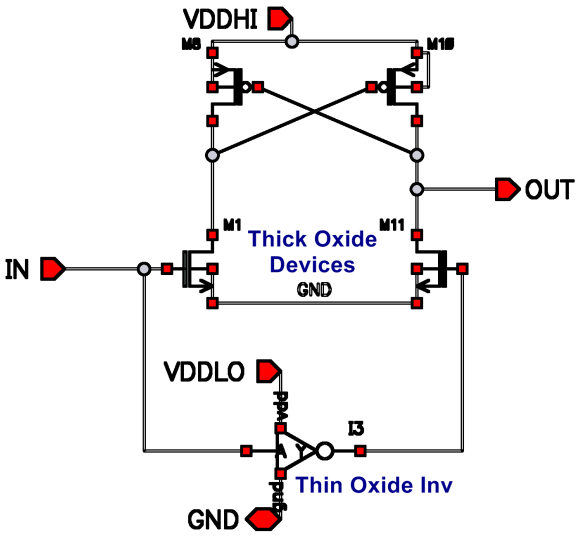


**Figure 3.8: 1-0V to 2-0V Regenerative Level Shifter –** Traditional level shifter with thick oxide devices provides transition of around 270ps as the bottom NNOS transistors must over power the PMOS latch. This is used in parts of the circuit where latency is not critical.

occupies 1.9x1.1mm$^2$. We used a more conservative design with high voltage breakdown option for capacitors, but standard breakdown would provide more than two times increase in capacitance for the same area. In addition, a custom inductor such as one used in [26] would likely lead to further efficiency improvement. To measure the efficiency we compared the power on input supplies and that delivered to a combination of on-chip and off-chip load with varying impedances. The ripple was observed via a 50-ohm matched line on a real time oscilloscope. In order to keep the ripple under the 100mV design target, the circuit automatically adjusts the number of CLCs based on loading condi-

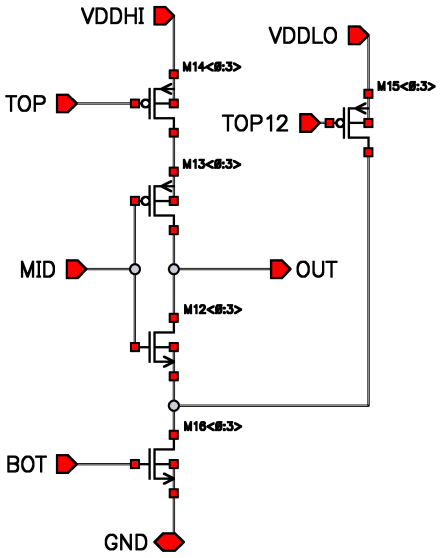


**Figure 3.9: Multi Level Driver With Thin Oxide Devices –** was designed to enable the middle PMOS and NMOS power fets' gates to be driven to either 0, 1 or 2V. It requires four independent inputs, which complicate the buffer strategy and require a custom logic decoder

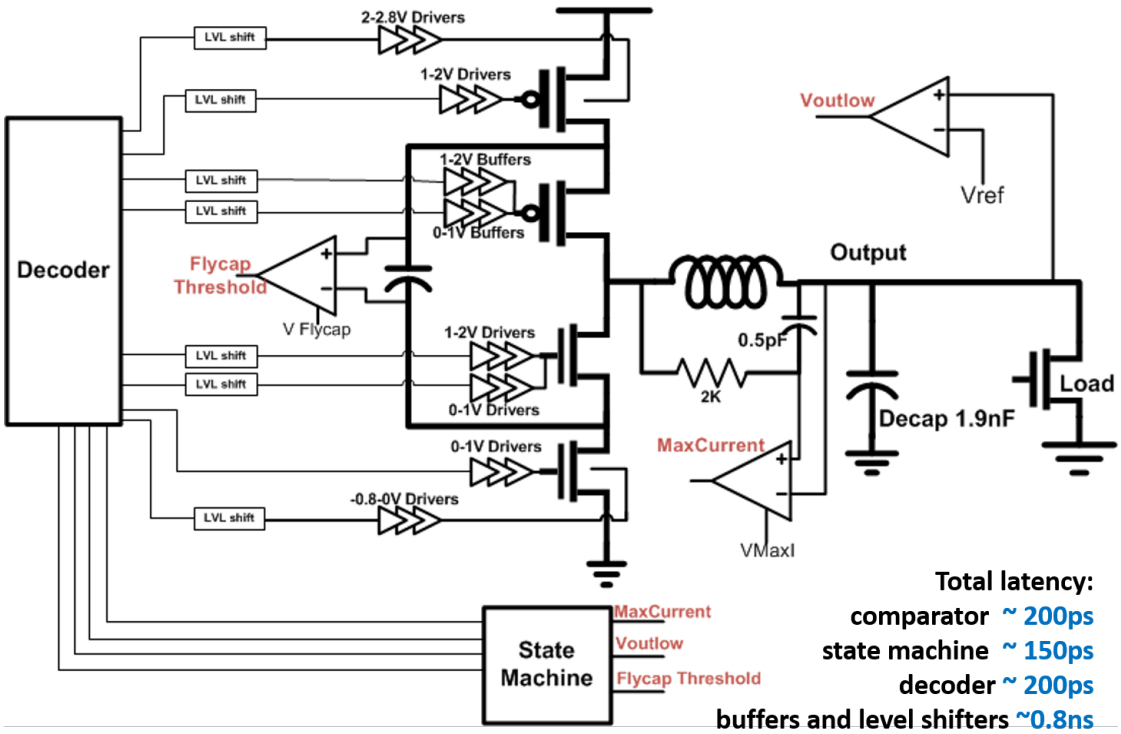


**Figure 3.10:** Full Block Diagram of the Power Stage Drive Strategy

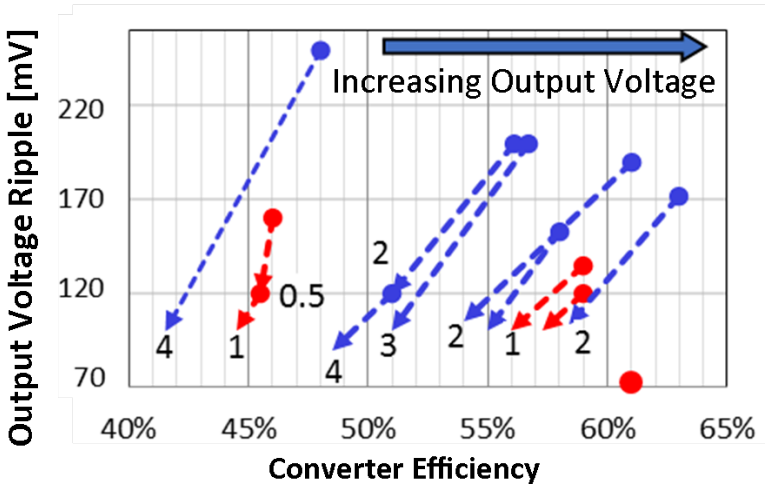


**Figure 3.11:** Measured ripple vs efficiency tradeoff for different number of current limited cycles (CLCs) relative to a quasi-resonant cycle. Circles represent non-current limited scheme. Blue: lighter load; red: heavier load.

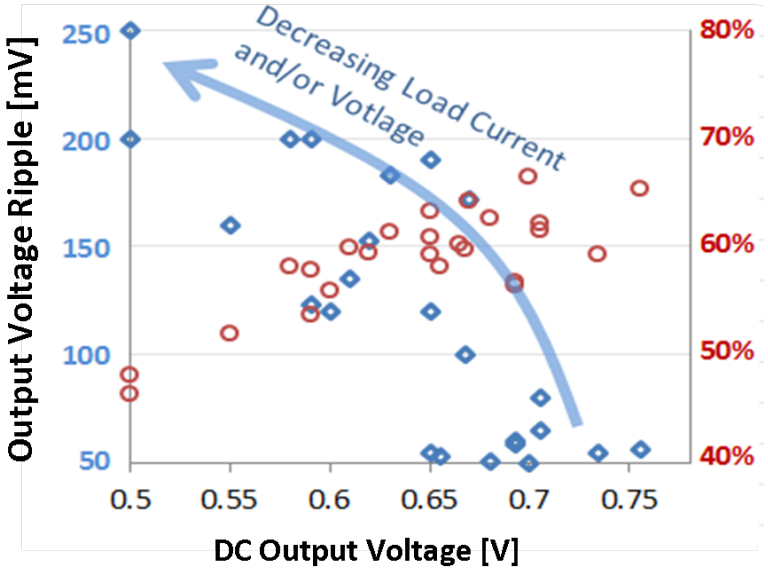


**Figure 3.12:** Measured output ripple (diamonds) vs. DC output voltage without current limiting for a 3-level converter for an input voltage of 1.8V across current levels. Circles represent the corresponding efficiency

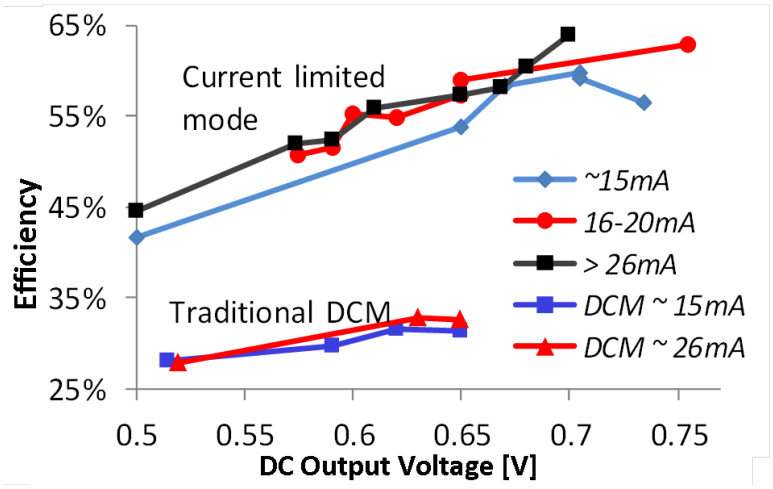


**Figure 3.13:** Measured efficiency results with part time resonant switching for 100mV ripple and same converter with traditional DCM mode

tions as indicated by the output voltage waveforms (Figure 3.14).The number of CLCs can also be changed by altering the Max Current Sense comparator offset thus influencing the current threshold through the inductor. Of course, adding CLCs, introduces slightly more switching and conduction losses. This tradeoff is illustrated in Figure 3.11. Further reduction in ripple can be achieved by an increase in output filtering cap. Even with the slight reduction in efficiency due to ripple control our scheme compares favorably to DCM, which has to operate at more than 3x the frequency increasing both switching and conduction loss (Figure 3.13). As noted in Equations 3.1 and 3.2 this additional switching and RMS conduction loss can be significant, and in this case accounts for a more than 60% improvement in efficiency across a range of low currents tested. In addition, this technique folds easily into existing designs of 3-level converters, and requires minimum alteration to the 3-level CCM topologies presented in [22]. Compared to other work in this area (Table 3.1), the addition of the light load operating mode makes 3-level converters even more appealing as a fully integrated solution for efficient step down even at steep ratios. Using this technique,

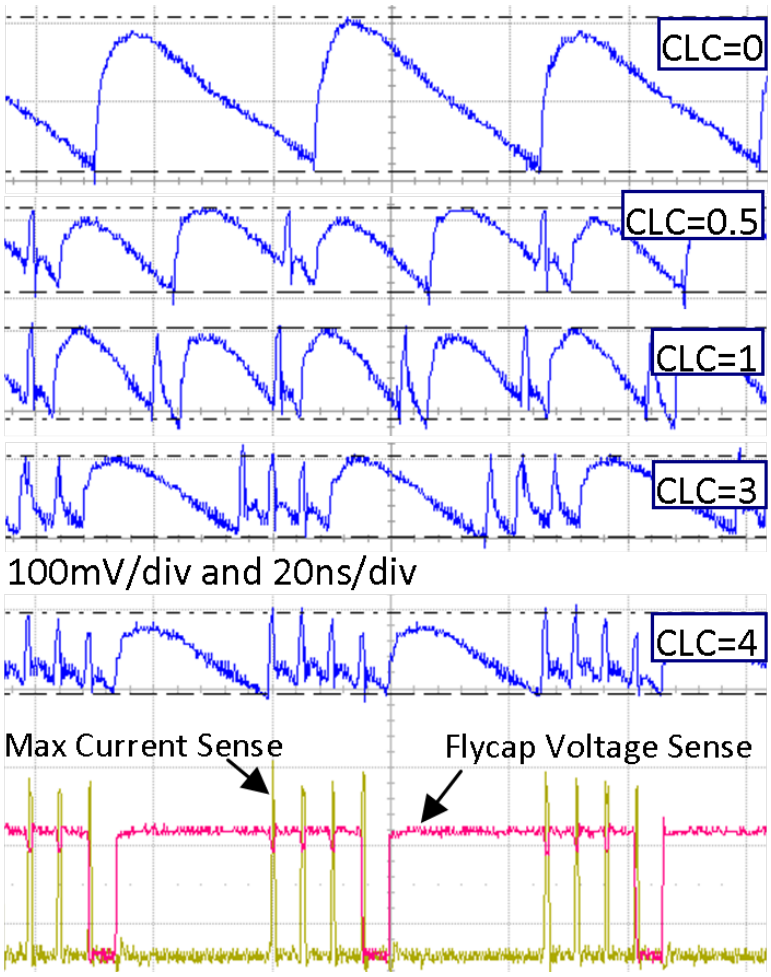


**Figure 3.14:** Measured output voltage ripple for different values of CLCs and example sense/control waveforms for CLC=4.

we are able to achieve the highest measured efficiency of integrated buck converter designs at high step down ratios and are able to support a wider range of currents than reported switched capacitor designs or 3-level converter designs. This improved performance for low voltages and currents is important for supporting the wide dynamic range required for DVFS and processor applications with extended sleep states.

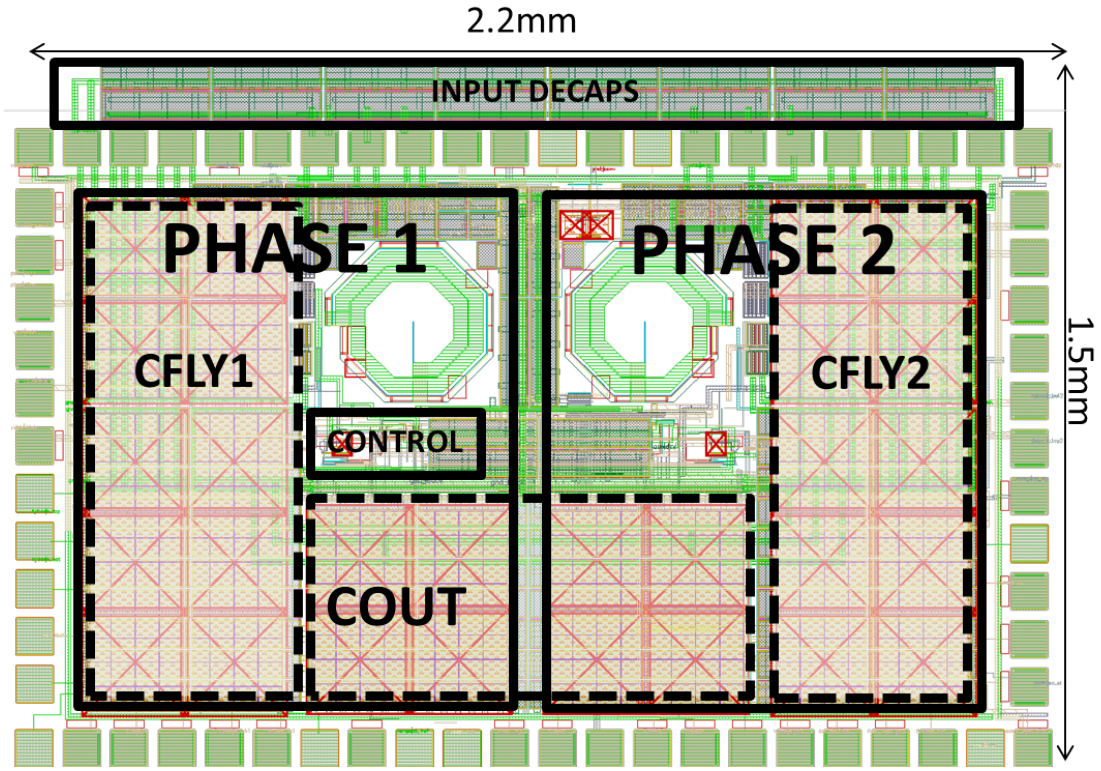


**Figure 3.15:** Layout and Floorplan of the 2 phase 3 level converter

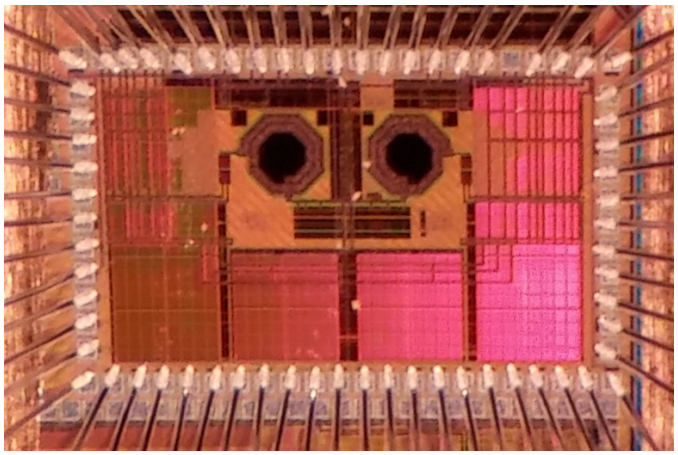

**Figure 3.16:** Photo of Wirebonded Fabricated Chip

| Reference | [52] | [26] | [29] | [19] | [49] | [22] | This work |
|---|---|---|---|---|---|---|---|
| **Topology** | Buck | Buck | S.C. | S.C. | 3 level* | 3 level | 3 level |
| **Technology [nm]** | 130 | 130 | 32 | 22 | 250 | 130 | 65 |
| **L/ph [nH]** | 3.9 | 2 | n/a | n/a | 26.7 | 1 | 1.5 |
| **Cfly/ph [nF]** | n/a | n/a | 0.125 | no info | 5 | 4.5 | 1.5 |
| **Cout [nF]** | 12.2 | 5 | n/a | n/a | 25.9 | 10 | 1.9 |
| **No. phases** | 4 | 1 | 32 | 4 | 1 | 4 | 2 |
| **Max current/ph [mA]** | 167 | 350 | 15.63 | 22 | 500 | 250 | 200 |
| **Min current [mA]** | 1 | 1 | no info | 1 | 1 | 100 | 1 |
| **Input voltage [V]** | 2.2 | 1.2 | 2 | 1 | 3.6 | 2.4 | 1.8 |
| **Conv. ratio** | 0.545 | 0.417 | 0.350 | 0.450 | 0.278 | 0.292 | 0.389 |
| **Eff at conv. ratio** | 56 | 55 | 62 | 63 | 65** | 50 | 64 |
| **Max ripple [mV]** | 120 | 60 | no info | 130 | 60 | >150 | 100 |

*bond wire/not fully integrated inductor, **simulated

**Table 3.1:** Comparison with other fully integrated converters for steepest conversion ratios achieved with >50% efficiency.

## 3.4 Conclusions

The results in the preceding sections suggest that it is possible to extend the efficient operation regime for a fully-integrated 3-level converter. The designed converter can operate from 15mA up to 150mA/phase with good efficiency for the target voltage range (0.55-1.1V). Additional phases can be used to increase the operating range on the high current end at the expense of area, but they do not help on the low end. The converter achieves about $0.2W/mm^2$, but this number would go up with possible improvements: a) embedding MOSCAPs underneath the inductor b) using denser, low voltage MOSCAPs in the design. Ultimately, the design is intended for a load that on average consumes about 100mA or more, but has extended sleep states that consume as little as 15mA. One of the problems that becomes apparent is that if the load demands less current, the converter design can not be easily reduced to accommodate that. The flyback capacitor area can be reduced, but this would necessitate higher switching frequencies due relative importance of L and C balance in the de-

sign (as explored in [50]). The inductor is already scaled to a smallest reasonable value. Further reduction of inductance would simply make its benefits discussed above negligible and result would turn into a poorly controlled SC converter.

The above argument suggest that a 3-level (or standard buck design for that matter) is best suited for larger loads or a conglomeration of loads operating at the same voltage. As will be discussed in the next chapter, it may be best suited as a Single-Adjustable-Frequency-Regulator (SAVR). In addition, the power density does not scale with process due to the inductor primarily relaying on good metalization. Back-end metals are typically standard across process generations and peak around 3um of top copper layer for advanced RF processes. On the other hand, the MOS capacitor density still improves down to 22nm node where it is expected to plateu at around $10fF/\mu m^2$. Further reduction might be impractical due to increase in gate leakage currents. This technological considerations further motivate investigation of SC converters for a more modular and flexible on-chip power supply delivery network.

# Chapter 4

# Switch Capacitor Converters for Coarse and Fine Grain Voltage Domains

As discussed in Section 3.4, the 3-level topology has certain short comings which would make it unsuitable for the target system described in 4.1.1. In addition, capacitor based switch mode converters benefit substantially from process scaling. Figure 4.1 shows the predicted improvement for 22nm designs. The improvement in efficiency or power density of the converter comes from improvement in MOSCAPs density (from 8fF to 11fF/$\mu m^2$) and from reduced $R_{on}$ of the switches per gate area. Note that a 3-level design would also benefit from this scaling, but not to the same extent as a switched capacitor converter as the inductor essentially remains the same. Thus, we now explore the design space and organization of on-chip switched capacitor based converters for multiple loads.

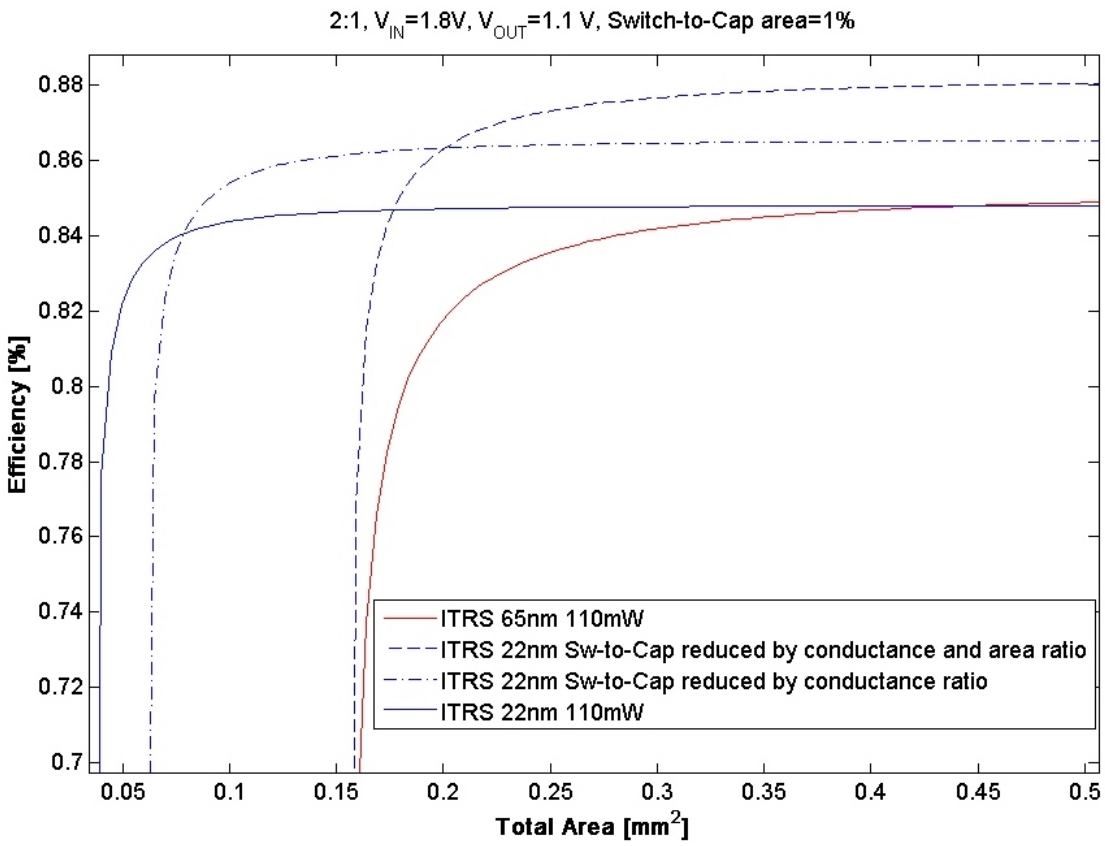


**Figure 4.1: Switch Capacitor Converter Scaling based on ITRS models –** Based on predicted ITRS roadmap models, future SC converter implementations will see significant performance improvements due to better switches and denser MOSCAPs. The blue lines represent model predictions for various design points in 22nm compared to a 65nm baseline design: area optimized for same efficiency as 65nm (solid), efficiency optimized for same area as 65nm(dash) or a combination of the two (dash dot).

## 4.1 On-Chip Switched-Capacitor PDNs

An SC power distribution network (PDN) for a chip multicore processor is constructed from one or more on-chip SC regulators combined with on-chip interconnect, power gating logic, and possibly additional control circuitry. Figure 4.2 shows five possible versions of an on-chip PDN. In Figure 4.2(a), a single fixed SC regulator is used to provide power to all cores at a common voltage. In Figure 4.2(b), per-core adjustable SC regulators can enable fine-grain voltage

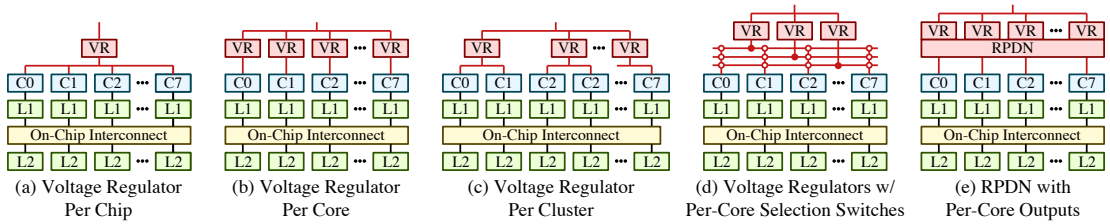


**Figure 4.2: Power Distribution Network Configurations for Multicore Processors –** Voltage regulators can be off- or on-chip to enable voltage scaling for cores and L1 mem system; additional regulators can enable voltage scaling for network and LLC. C = core; L1 = L1 mem system; VR = voltage regulator; L2 = L2 cache; • = power supply fixed connection; ○ = power supply selection switch. *Courtesy of Christopher Batten*

scaling at large area overhead, and in Figure 4.2(c) this overhead is amortized by grouping cores into shared voltage islands at the expense of voltage scaling flexibility. In Figure 4.2(d), a small number of fixed SC regulators provide a set of fixed voltage levels and power MOSFETs choose an appropriate level for each core. Finally, Figure 4.2(e) illustrates how an RPDN is tightly integrated with small per-core SC regulators to enable flexible reconfiguration of energy storage on demand. In this thesis, we focus on the PDNs shown in Figures 4.2(a,b,e). RPDNs integrate similar functionality to the regulator shown in Figure 4.2(d) with reduced area overhead since RPDNs have added flexibility and each regulator does not need to be independently provisioned for the worst case loads. Similarly, Figure 4.2(c) presents an interesting middle ground but reduces flexibility when compared to Figures 4.2(b,d,e) while requiring some area overprovisioning relative to Figures 4.2(d,e).

In this section, we first sketch our target system and then analyze four potential PDNs: single fixed-voltage regulator (Figure 4.2(a)), single adjustable-voltage regulator (Figure 4.2(a)), multiple adjustable-voltage regulators (Figure 4.2(b)), and RPDNs (Figure 4.2(e)).

### 4.1.1 Target System

The design of a specific PDN will depend heavily on the target system that will use the regulated output power. Although much of our analysis is applicable to larger high-performance systems, we chose to focus on the smaller low-power systems that will likely be the first to integrate significant on-chip voltage regulation. Our target system is an embedded processor composed of: eight in-order, single-issue, RISC cores; private, coherent 16 KB instruction and data L1 caches; and a shared 512 KB unified L2 cache. We have implemented the core and L1 memory system for this design in RTL and used a commercial standard-cell-based ASIC CAD toolflow targeting a TSMC 65 nm process to generate layout for one core and the associated L1 memory system. We assume the external supply voltage is 2 V (it is typically used to power I/O circuits on chip anyways) and that fine-grain voltage scaling should provide at least four voltage levels: 0.9 V for the nominal supply voltage; 0.6 V for a slow, low-power execution mode (which we call *resting mode*); 1.05 V for a fast, high-power high-power execution mode (sprinting mode); and 1.2 Vfor an even faster execution mode *super sprinting mode*). Analysis of the placed-and-routed design indicates each core is approximately 0.75 $mm^2$ and can run at 333 MHz at 0.8V. We predict that more aggressive RTL and circuit design could increase this clock frequency by 2x or more.

First-order estimates suggest the full eight-core system would be approximately 0.75x8=6 $mm^2$. When running a reasonable workload, each core/L1 consumes approximately 25 mW, and when idle (e.g., waiting for work or a synchronization primitive), each core/L1 consumes approximately 3 mW. This implies that the power for all eight cores and L1 memory system (excluding the

L2 cache) can range from 100-200 mW and that the peak power density of the cores and L1 memory system is approximately 0.05 W/mm$^2$. For all designs we assume (potentially multiple) on-chip phase-locked-loops (PLLs) to enable fast frequency adjustment based on recent low-power designs [9, 13]. We will use these target numbers to help drive the design of each PDN.

### 4.1.2 DVFS Plan

| Supply Voltage | Frequency | Dyn. Power - Calculated | Power - Simulated |
|---|---|---|---|
| 1.2 | 126% | 181% | 205% |
| 1.1 | 114% | 137% | 146% |
| 1 | 100% | 100% | 100% |
| 0.9 | 85% | 69% | 66% |
| 0.8 | 69% | 44% | 41% |
| 0.7 | 52% | 25% | 23% |
| 0.6 | 34% | 12% | 11% |

**Table 4.1: Dynamic Voltage and Frequency Scaling (DVFS) Plan from simulated FO4 inverter delay in 65nm Technology –** Calculated power according, to $P = CfV_{dd}^2$ is very close to simulated power. Small discrepancy is likely due to shoot-through current when both PMOS and NMOS conduct during switching

The gate level cell libraries are only characterized at two voltages and the RTL synthesis only provides power and frequency at one point. However, an accurate estimation of core frequency with changing $V_{dd}$ is critical for our application, as it directly impacts performance and power consumption. Therefore, we use SPICE-level simulations to determine the scaled clock speeds for each supply level on each core within the processor. We use 13 delay stages consisting of multiple FO4 loaded inverters, NAND, and NOR gates connected in a loop configuration, such that the total delay in the loop matches our RTL frequency for a given voltage. We then observe the change in output frequency

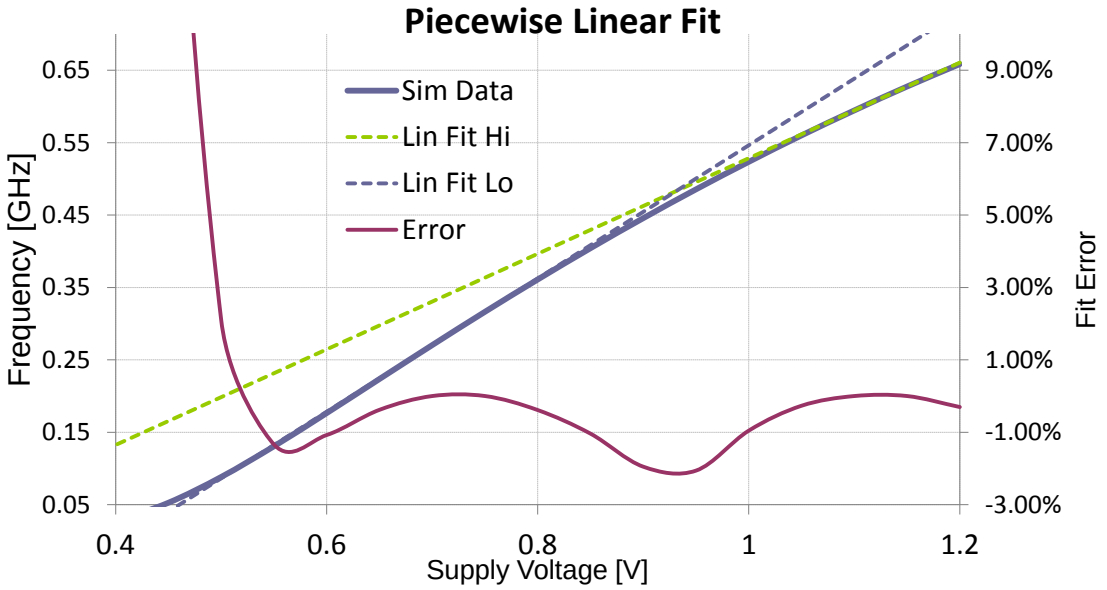


**Figure 4.3: DVFS Piecewise Linear Fits and Error for 65nm –** A single linear or quadratic fit did not work across the range of interest. Best results were obtained with a piecewise linear fit, taking the minimum of Fit Lo and Fit Hi fitted each individually to the bottom and top portion of the simulated data respectively. The coefficients are as follows: $F_{LO} = 9.28e8V_{dd} - 3.84e8$ and $F_{HI} = 6.40e8V_{dd} - 1.14e8$

with supply voltage as a model for the change in delay for a similar logic stage. The results for the relative frequency and power changes from SPICE transient simulation are shown in Table 4.1. Note that the ratio of the extreme power points in the target range is 18x with a corresponding 4x ratio in frequency, so the impact of DVFS on system power and performance is enormous. Using a single linear or quadratic frequency scaling model did not produce a good fit in the voltage range of interest between 0.6 and 1.2V. Best fit was obtained by taking a minimum of the combination of two linear fits with the error being less then 2% across the range of interest as seen in Section 4.3. Once below 0.6V, the error increases dramatically; quadratic relationship would have to be employed in this range as $V_{dd}$ gets closer to the threshold voltage of the process.

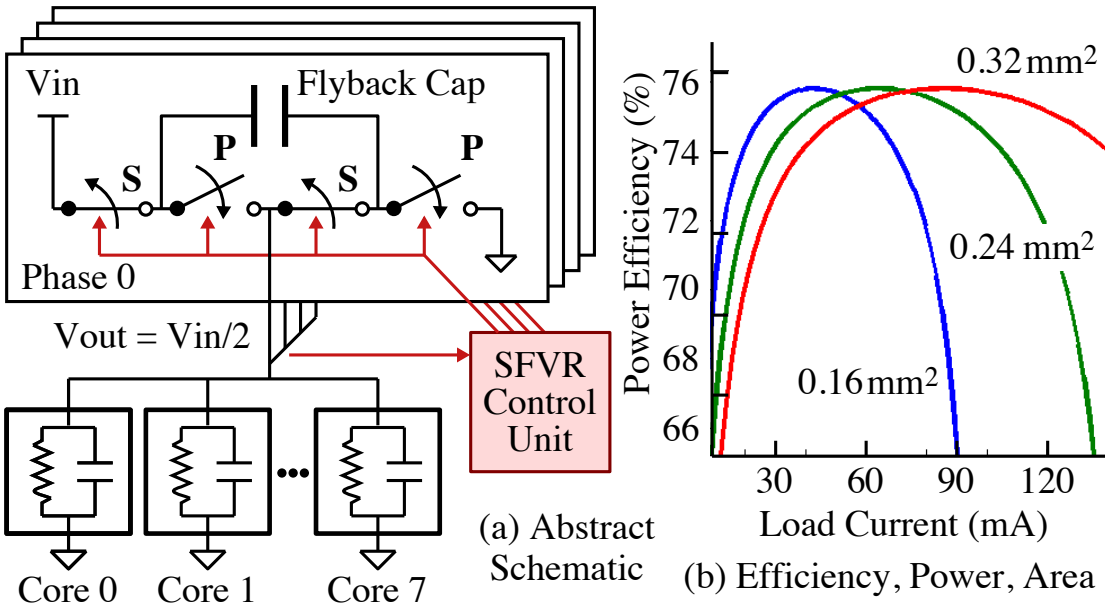


**Figure 4.4: SFVR –** (a) 2:1 topology converts Vin to Vin/2 for eight cores; S = switches closed during serial mode; P = switches closed during parallel mode; control unit monitors Vout to regulate switching frequency; 16 phases are included to reduce ripple (only four phases shown for simplicity). (b) power efficiency varies as a function of output power and flyback capacitance area. *Schematic diagram thanks to Christopher Batten*

## 4.2 Organization of Voltage Domains

In the previous section, we established the target eight-core system, which effectively consists of eight dynamic loads. The power consumption of each load varies according to the DVFS plan outlined, but also depends on particular workloads scheduled for each core. The area of each core is known form the RTL synthesis and we can now proceed to consider various PDNs for this system along with the benefits and overheads they provide.

### 4.2.1 SFVR: Single Fixed-Voltage Regulator

A single fixed-voltage regulator (SFVR) provides a useful baseline to compare against more sophisticated PDNs. Figure 4.4(a) illustrates a basic 2:1 switched-capacitor design. In *series mode*, the flying and load capacitance are connected in series, and the input voltage supply charges up the the flying capacitor. In *parallel mode*, the flying and load capacitance are disconnected from the input voltage supply and connected in parallel; the flying capacitor acts as an energy source that is discharged into the load to supply power to the core. As the converter switches between the series and parallel modes, the output voltage will gradually converge to be half the input voltage. Faster switching frequencies reduce voltage ripple but decrease efficiency due to switching losses; larger flying capacitors require more area but can enable slower switching frequencies for the same load current increasing efficiency as they can hold more charge. Figure 4.4(b) illustrates this trade-off using an analytical circuit-level model. As the total area of the regulator increases, the curve moves to the right and broadens, indicating higher efficiencies can be achieved at higher powers and over a wider range of operating conditions. The switching frequency can also be used for fine-grain control of the output voltage; a SFVR control unit monitors the output voltage and adjusts the switching frequency in response to varying current loads in order to maintain a constant output voltage. Realistic switched-capacitor regulators almost always include support for switching multiple phases of the signal in parallel to further minimize ripple. We explore the SFVR design space for our 65nm CMOS process and find a reasonable design that can provide 75% power efficiency with an area of $0.24\,mm^2$ (4% of the core/L1 area). As noted previously, for a switched capacitor regulator with many phases, it may be possible to repurpose the mandatory on-chip decou-

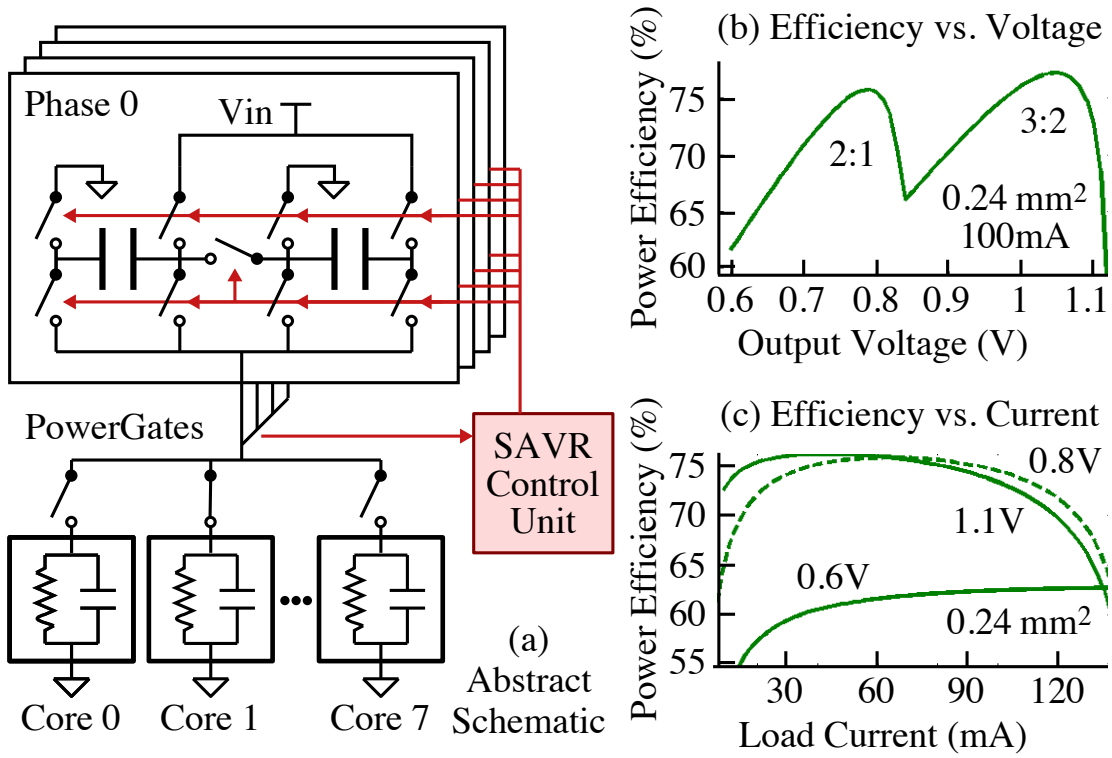


**Figure 4.5: SAVR –** (a) control unit can configure flyback capacitance to convert Vin to Vin/2, 3Vin/2, or Vin/3; other intermediate voltages are possible by adjusting the regulation frequency; 16 interleaved phases are included to reduce ripple (only four phases shown for simplicity). (b) power efficiency varies as a function of the target output voltage. (c) power efficiency also varies as a function of load current at a given target output voltage. *Schematic diagram thanks to Christopher Batten*

pling capacitance as flying capacitance for the switching regulator, helping to reduce the area overhead [29].

### 4.2.2 SAVR: Single Adjustable-Voltage Regulator

Although SVFR is simple and compact, it cannot exploit fine-grain voltage scaling. Figure 4.5(a) illustrates a single adjustable voltage regulator (SAVR) that can output a range of voltages from 0.6–1.1 V and thus enables temporal fine-grain voltage scaling. This SC regulator uses a more complicated flyback capacitor topology to enable three input/output ratios. Because this regulator must

support all possible operating conditions for the multi-processor, it is designed for high efficiency even at the highest power levels, a condition that requires a larger overall regulator in terms of capacitor area than the nominal or resting conditions. The SC regulator achieves the highest efficiency at these discrete ratios (0.6 V@2:1 = 56%, 0.8 V@2:1 = 72%, and 1.1 V@3:2 = 75%) although it is also possible to output other target voltages with a linear decrease in efficiency (see Figure 4.5(b)). Note that the power efficiency also varies with current at a given target output voltage (see Figure 4.5(c)). Cores can potentially run in resting mode when their performance is not critical to the overall application performance (e.g., waiting on a long-latency cache miss or waiting for work) or run in sprinting mode when their performance is critical to the overall application performance (e.g., executing sequential code or a critical section, lagging behind other cores). Note that all eight cores cannot run in sprinting mode without exceeding a reasonable chip-wide power limit, so sprinting is only possible when some cores are power gated.

### 4.2.3 MAVR: Multiple Adjustable-Voltage Regulators

While SAVR offers the flexibility to achieve fine grain voltage regulation in time, it requires that all cores be regulated to the same supply voltage at any given instance in time. This does not allow the system flexibility to achieve the benefits of dynamic voltage scaling across cores. Adding this functionality requires per-core regulation like that shown in Figure 4.2(b). This SC regulator network is composed of per core voltage regulators, each designed using the more complicated flyback topology used in SAVR to support multiple operating voltages and power conditions. Each MAVR converter operates with many phases and together with each core forms a individual unit that is agnostic to power con-

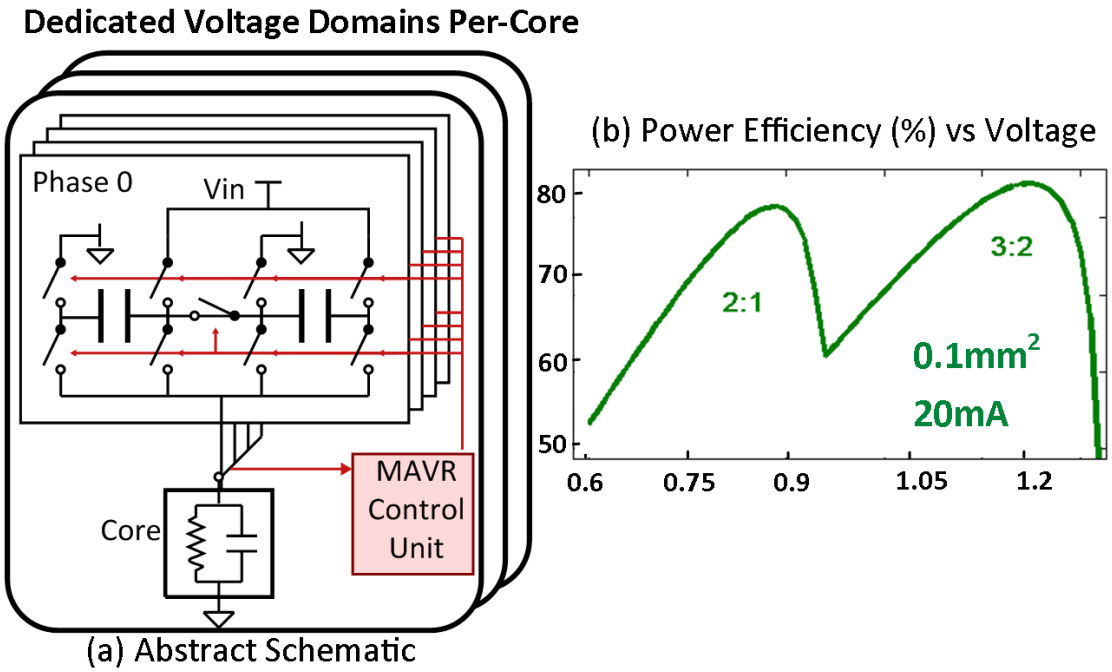


**Figure 4.6: MAVR –** (a) control unit can configure flyback capacitance to convert Vin to Vin/2, 3Vin/2, or Vin/3; other intermediate voltages are possible by adjusting the regulation frequency; 16 interleaved phases are included to reduce ripple (only four phases shown for simplicity). (b) power efficiency varies as a function of the target output voltage. *Schematic diagram thanks to C. Batten*

sumtion or voltage of other such units as shown in Figure 4.6. In this design, each per-core regulator is designed to have an area of 0.1 $mm^2$ based upon the results of the analytical efficiency model shown in Figure 4.9. This large area is required in order to achieve efficient regulation in even the high-power case for each regulator, thus allowing compiler/programmer to remain agnostic to the voltage regulation hardware. Designing for this operating point not only consumes area, but also reduces the efficiency in the low-power resting mode, since larger capacitors suffer from greater leakage as shown at the low power end of the curve in Figure 4.9. In addition to the area overhead of MAVR, there is also execution time overhead due to the transient response of level switching shown in Figure 4.10. In order to switch between different power levels, the feedback loop of the regulator must adjust the switching speed of the regulator

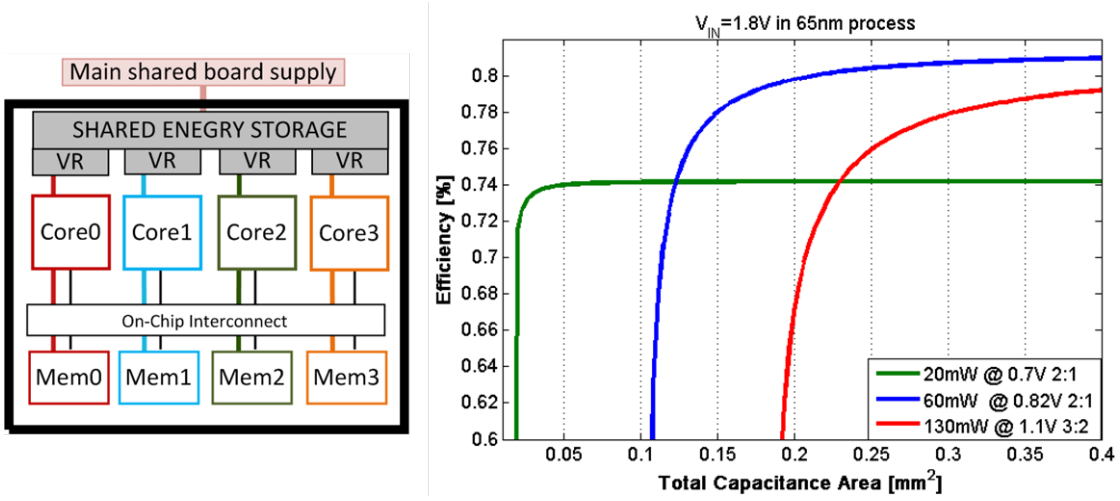


**Figure 4.7: RPDN Conceptual Diagram and Capacitance Over-provisioning –** The larger the output power of the converter, the more capacitance is required for efficient operation. Shared energy storage (in this case capacitance) concept diagram on the left.

to accommodate this change. This frequency adjustment causes the regulator to settle to its steady state output voltage over some loop adaptation time. In the case of MAVR this time can be more than 1 µs, as in the case shown where the regulator switches from nominal to sprinting.

### 4.2.4 RPDN: Reconfigurable Power Distribution Networks - Concept

Clearly a significant design challenge in per-core voltage regulation is how to support multiple supply levels without over-provisioning the per-core regulators. This is particularly important since the system will not typically support every core sprinting at the same time, due to thermal and power constraints. MAVR requires that each pre-core regulator independently support sprinting mode. The efficiency vs capacitance area plot in Figure 4.7 show that the area required to support efficient conversion increases dramatically with output power

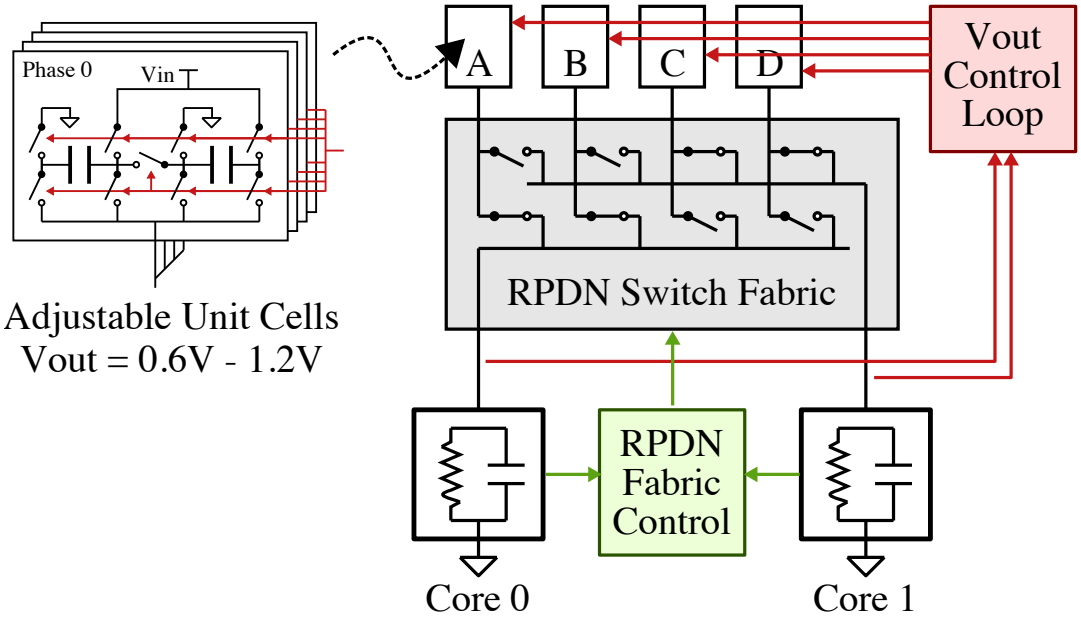


**Figure 4.8: RPDN Potential Implementation With Adjustable Unit Cells –** All unit cells are designed for an adjustable output voltage from 0.6–1.2 V; unit cells A and B are powering core 0; unit cells C and D are powering core 1. Each core has a dedicated control loop. Each cell has power switches to assign output to a particular core and clock input mux to select the corresponding control loop

that the converter provides. Conversely, when low output power is required, very little area is necessary for efficient operation. This is the key insight behind RPDN. In order to mitigate MAVR's area overhead we propose RPDN as a mechanism for allowing per core regulation while sharing the large energy storage elements across regulators, as shown in Figure 4.7. This way, when one core is sprinting, it can greedily borrow capacitance from other regulators in resting mode to improve overall efficiency.

Figure 4.8 illustrates a simple example RPDN for two cores. The *RPDN control unit* configures the *RPDN switch fabric* to connect *RPDN unit cells* to supply power to each of the cores. In this example, each RPDN unit cell is a small switched-capacitor 2:1 regulator and the RPDN switch fabric is a two-input, two-output crossbar. In nominal mode, the RPDN switch fabric is configured

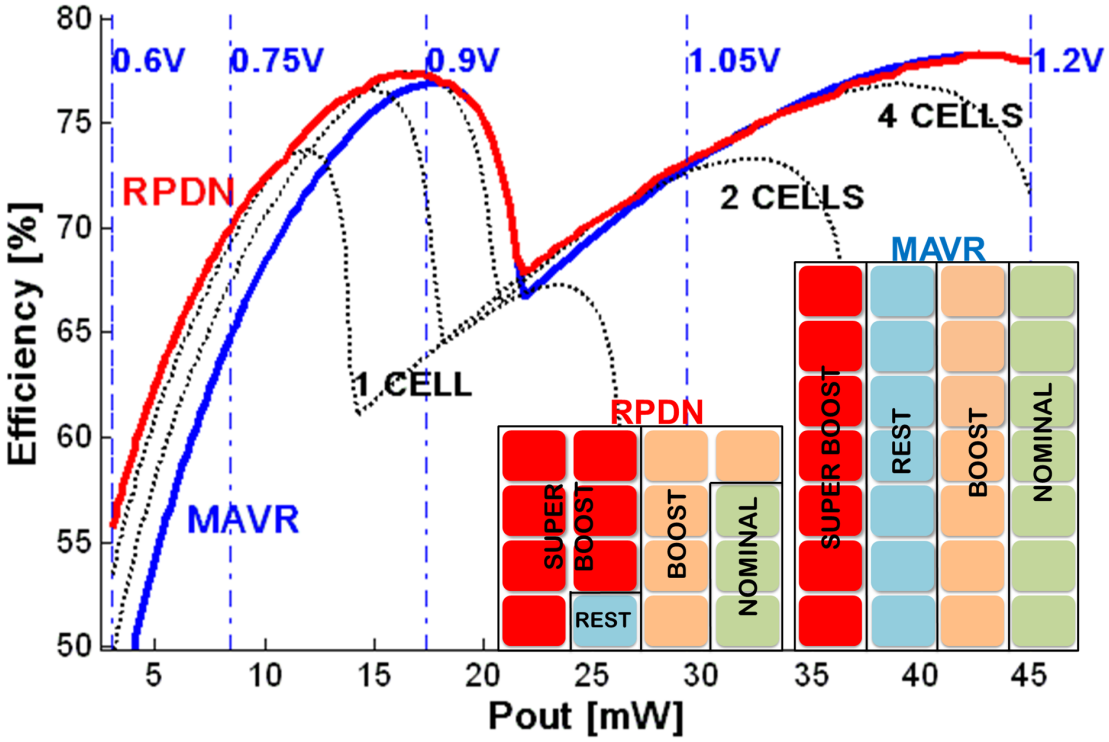


**Figure 4.9: MAVR and RPDN Power Efficiency vs. Output Power per Core –** RPDN tracks best possible efficiency while maintaining lowest area. MAVR efficiency drops at lower power as loses due to leakage become a more significant portion of output power. RPDN cell efficiencies for unit cell of 0.015 $mm^2$ for 1, 2 and 4 cells in parallel are also shown. Inset shows sample area utilization and relative size of MAVR compared to RPDN where each of cores is operating in a distinct mode (rest, nominal, sprint, and super-sprint). RPDN shows corresponding cell allocation.

such that regulators A and B supply core 0 and regulators C and D supply core 1. If core 0 is idle while core 1 is sprinting, the RPDN switch fabric can be reconfigured such that regulator A continues to supply a lower voltage and current to core 0 while regulators B–D supply a higher voltage and current to core 1. The design in Figure 4.8 is greatly simplified to illustrate the basic concept of RPDNs. Our actual RPDN design includes eight cores, 32 unit cells, and eight phases per cell. Preliminary estimates showed that scaling the RPDN switch fabric across all eight cores incurred significant losses, so the RPDN is partitioned into two sub-RPDNs with each RPDN operating in a relatively isolated

fashion to manage four cores. Each sub-RPDN has half of the 32 unit cells to distribute to its respective four cores. Each unit cell uses the more sophisticated multi-level SC regulator design that enables both 2:1 and 3:2 step-down conversions similar to the regulator shown in Figure 4.5(a) except with only eight phases. Based on 65 nm transistor-level models, the power switches introduce a 0.5% efficiency degradation with a negligible 2% extra converter area. More details can be found in Sec. 5.3 and Sec. 6.3.1

The RPDN architecture offers obvious advantages in terms of area savings. Based on analytical model developed by Seeman [43] and augmented to include the effect of leakage, we compute the relative area and efficiency for each case described. These results, shown in Table 4.2, indicate an area savings of 40% over MAVR (see Figure 5.6) to support per core supply regulation across the same number of cores. Other advantages exist as well. At low power, regulators can be configured for lower capacitance, improving the efficiency at the low end by reducing the impact of leakage. As a result, RPDN is able to achieve the maximum efficiency across the range of SC converter designs as shown by the solid line in Figure 4.9. Furthermore, because each converter has the flexibility to change not only the SC divide ratio, but also the capacitance associated with that voltage and power level, this impacts switching transients. In the MAVR and SAVR cases, when a regulator moves from nominal to sprinting mode, the feedback loop must adjust the switching speed up quite a bit to accommodate the new power level. Alternatively, in the RPDN case, adjusting from nominal to sprinting mode will adjust both the voltage level and the capacitance, requiring the feedback loop to make a much smaller change in switching speed. These predictions were verified by a spice level simulation with a

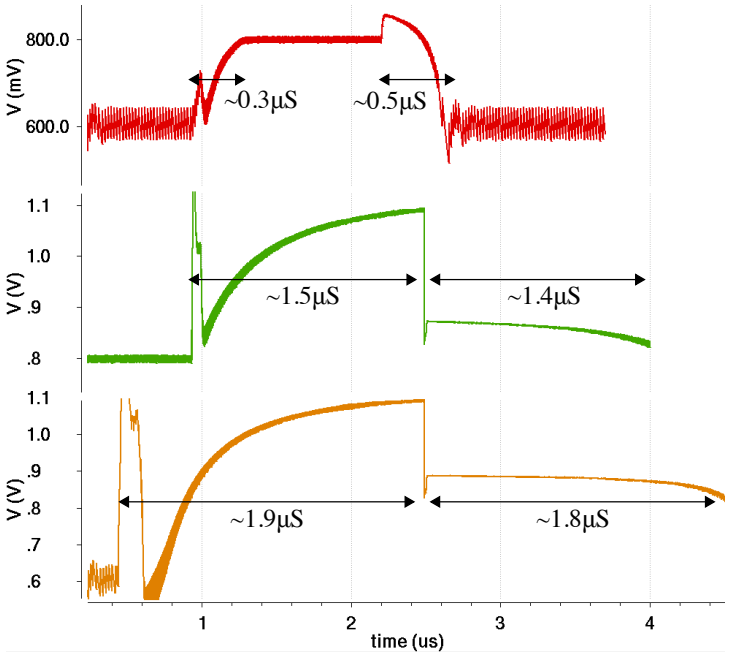


**Figure 4.10: MAVR Transient Response –** Transistor level transient simulation of the MAVR design with fixed capacitance per core. Response times vary from 0.3–1.9 µs.

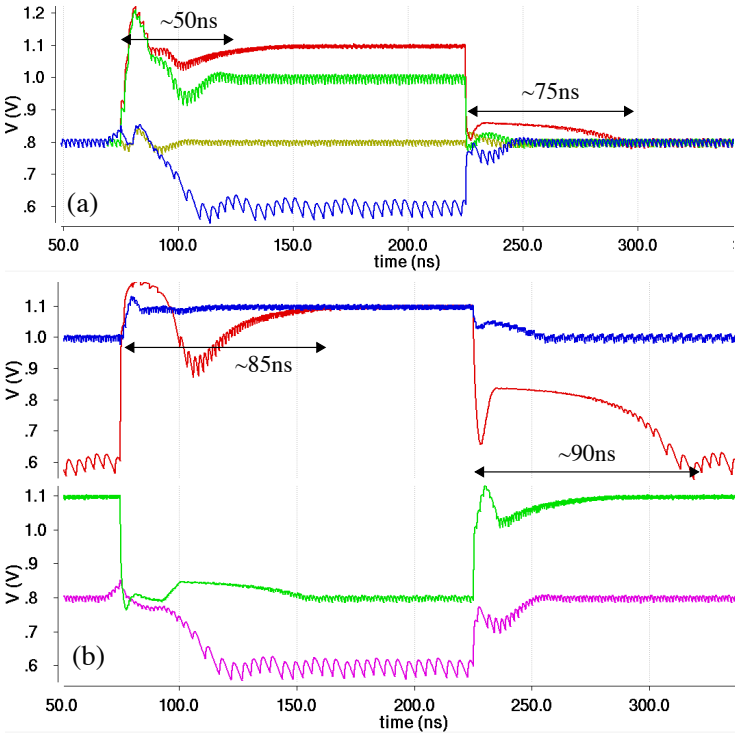


**Figure 4.11: RPDN Transient Response –** Four-core sub-RPDN design with capacitance reallocation: (a) all cores start at nominal and move to four distinct levels and than back to nominal; (b) barious cases, including worst case from sprinting to resting modes.

| | PDN Area ($mm^2$) | Eff Decap ($mm^2$) | Area Overhead ($mm^2$) | Area Overhead as Perecent of Core Area | | |
|---|---|---|---|---|---|---|
| | | | | $P = 0.05$ | $P = 0.15$ | $P = 0.25$ |
| **S*VR** | 0.24 | 0.12 | 0.12 | 2% | 6% | 10% |
| **MAVR** | 0.80 | 0.40 | 0.40 | 7% | 30% | 57% |
| **RPDN** | 0.48 | 0.24 | 0.24 | 4% | 14% | 30% |

**Table 4.2: Comparison of PDN Area Overhead –** S*VR = SFVR and SAVR have similar overheads. Core area assumed to be $6mm^2$. First three columns assume a core power density of $0.05\,W/mm^2$. Final three columns extrapolate area overheads as a function of core power density ($P$). Since SC provides effective decoupling cap, overhead is just area required beyond what would have already been required for 10% decoupling cap. For this design, beyond $0.05\,W/mm^2$ the converter area exceeds the decap area, thus reducing this overhead is critical.

| | PDN Area | Power Efficiency for Vout = | | | Transient Response (ns) | | | Voltage Scaling | |
|---|---|---|---|---|---|---|---|---|---|
| | ($mm^2$) | 0.6V | 0.8V | 1.1V | Min | Typ | Max | Space | Time |
| **SFVR** | 0.24 | n/a | 75% | n/a | n/a | n/a | n/a | No | No |
| **SAVR** | 0.24 | 56% | 72% | 75% | 70 | 250 | 480 | No | Yes[1] |
| **MAVR** | 0.80 | 51% | 73% | 73% | 360 | 900 | 1850 | Yes | Yes |
| **RPDN** | 0.48 | 62% | 75% | 74% | 30 | 70 | 170 | Yes | Yes |

**Table 4.3: Comparison of PDNs –** Roughly organized in increasing complexity, capability, and performance. [1]SAVR sprinting mode is only possible if idle cores are power gated.

verilog-a based model of the frequency loop reflecting individual blocks of the loop.

The result, as can be seen in Figure 4.11, is that for each case of adjusting the regulator over a four core RPDN, the transient time to adapt to steady state is less than 150nS, more than an order of magnitude faster than the transient response for MAVR as shown in Figure 4.10.

## 4.3 Summary of SC Regulator Configurations

Tables 4.2 and 4.3 summarize the tradeoffs discussed in the previous sections. While on-chip voltage regulation offers the potential for fast, flexible control, it also incurs various overheads. In the case of SFVR, no flexibility is offered. SAVR offers some flexibility in time, with longer transient times to reach each steady state regulation voltage, however all cores must be regulated together, reducing the ability to independently optimize threads in a multi-threaded application. MAVR increases the flexibility for fine-grain voltage scaling, but at a high area overhead, reduced efficiency across the operating range, long response times. Finally, RPDN offers an interesting middle ground. RPDN enables the flexibility of MAVR with significantly reduced area overhead, improved efficiency across the operating range, and faster transient adaptation.

## 4.4 PDN Impact on Eight-core System Performance

In this section we analyze the impact of PDNs on the system level performance and power. As mentioned in Section , single-threaded workloads 41-64% speed up in execution time across benchmarks, simply due to boosted operating frequency of the core. This improvement comes are various power overheads depending on PDN type, used as seen on the Figure 4.12. RPDN offers the lowest power due higher efficiency compared to MAVR at low powers thanks reduction in leakage. Next we consider RPDN impact on energy efficiency and speed up for multi-threaded workloads. In Section 1.2.2 parameter sweeps for different characteristics of a PDN set minimum design targets that achieve best performance gains. Figure 4.13 shows simulation results for same applications

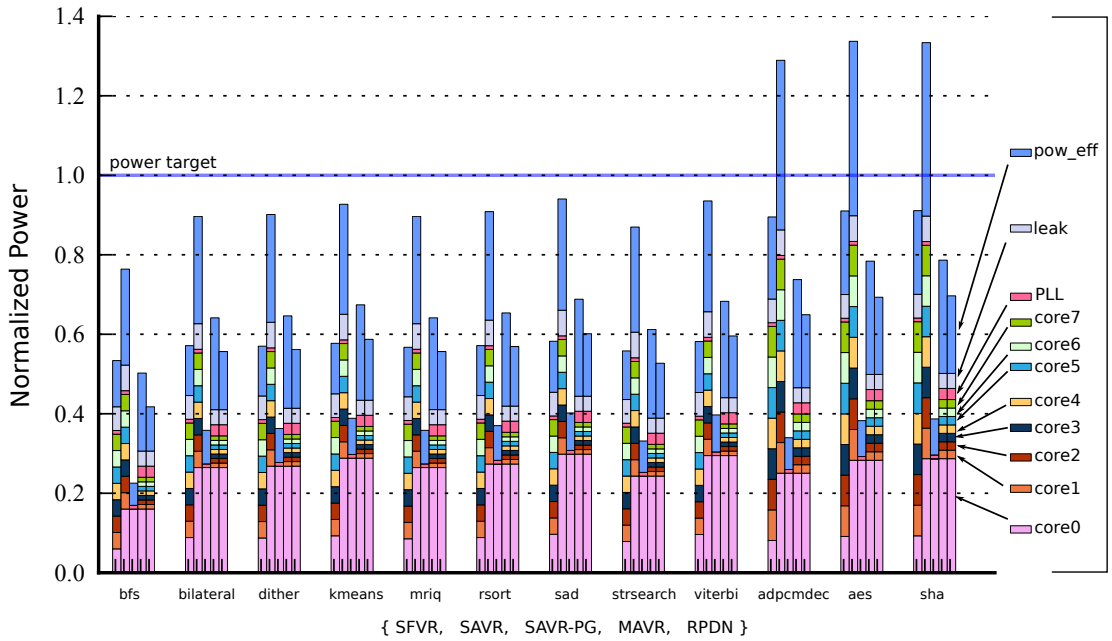


**Figure 4.12: Breakdown of Power for Single-threaded applications for Various PDNs–** The blue area represents power lost in the regulator and there are also leakage and PLL components as well as contributions from various cores. The cases from the left are as follows: 1) Baseline - all cores at nominal voltage of 0.8V - no performance improvement 2) All cores at 1.1V boost voltage , including cores 1-7 which aren't doing useful work 3) Cores 1-7 are power gated - this power saving technique is orthogonal to fine grain DVFS explored in this work and can result additional latency not modeled here 4) Independent core supply voltage regulators allow core 0 to run at 1.1V and others at 0.6V to save energy 5) Improved version of (4) presented in this work in Section 4 using Reconfigurable Power Distribution Networks which also consumes 40% less area. **results generated by Christopher Torng using cycle level simulator with converter efficiency data*

on the target system (Section 4.1.1) including the realistic overheads for PDN considered in chapter 4. Even though RPDN shows higher normalized power for some of the applications, it is actually more energy efficient since the task is competed faster compared to MAVR and shown in the normalized energy efficiency plot in Figure 4.14 and in Table 4.4. Applications with a lot of transitions such as viterbi and dither show reduced contribution to 'transition' part of the overall power for RPDN as compared to MAVR. Thus RPDN shows a clear ben-

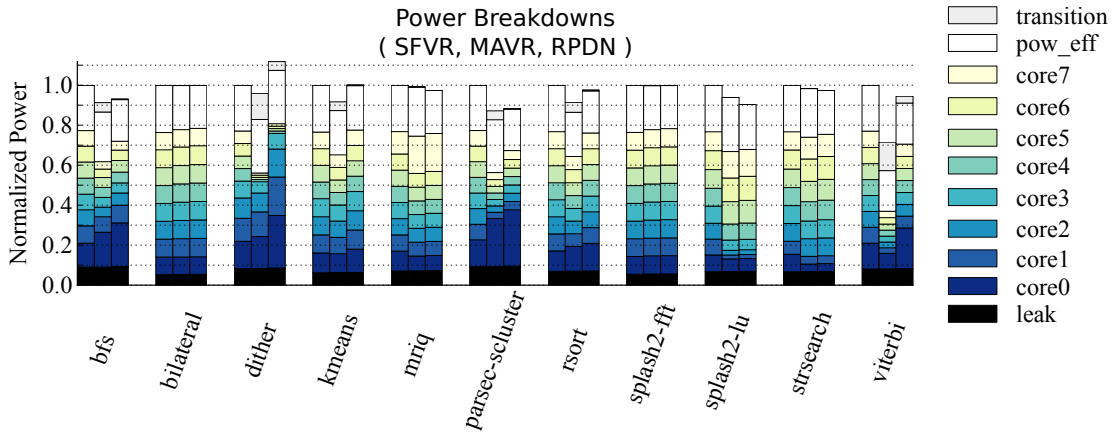


**Figure 4.13: System-Level Evaluation for SFVR, MAVR, and RPDN –** MAVR and RPDN power results all normalized to SFVR. "transition" is transition power overhead. "pow_eff" is regulator power efficiency overhead. "leak" is leakage power. **Architecture results thanks to Christopher Torng*

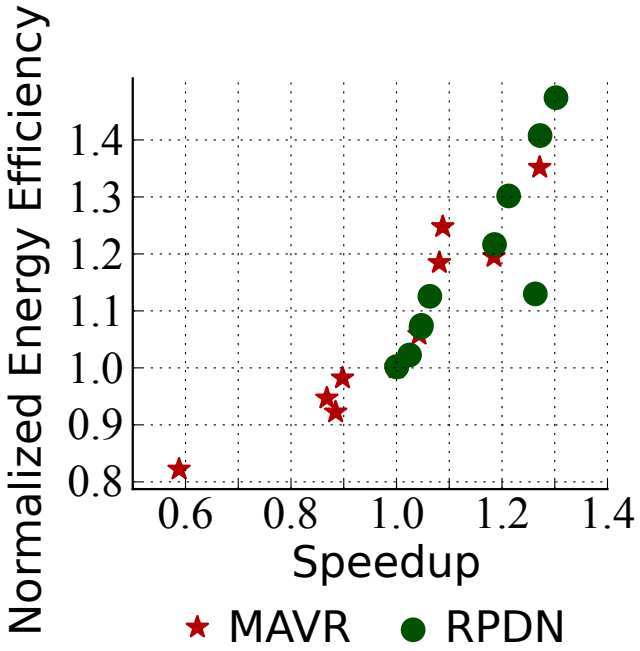


**Figure 4.14: System-Level Evaluation for SFVR, MAVR, and RPDN –** MAVR and RPDN energy efficiency vs speedup (performance) normalized to SFVR. **Architecture results thanks to Christopher Torng*

| App | # Voltage Transitions | SFVR Exec Time (us) | MAVR Speedup | RPDN Speedup | SFVR Energy (uJ) | MAVR $E_{norm}$ | RPDN $E_{norm}$ |
|---|---|---|---|---|---|---|---|
| bfs | 47 | 169 | 1.08 | 1.21 | 9 | 0.84 | 0.77 |
| bilateral | 11 | 4638 | 1.00 | 1.00 | 511 | 1.00 | 1.00 |
| dither | 3899 | 6238 | 0.88 | 1.26 | 412 | 1.08 | 0.89 |
| kmeans | 396 | 519 | 0.87 | 1.02 | 47 | 1.06 | 0.98 |
| mriq | 39 | 12342 | 1.18 | 1.19 | 993 | 0.84 | 0.82 |
| scluster | 244 | 67012 | 1.09 | 1.30 | 5203 | 0.80 | 0.68 |
| rsort | 205 | 341 | 0.90 | 1.05 | 26 | 1.02 | 0.93 |
| strsearch | 25 | 1601 | 1.04 | 1.05 | 335 | 1.00 | 1.00 |
| viterbi | 25924 | 7239 | 0.59 | 1.06 | 1612 | 0.74 | 0.71 |
| splash2-fft | - | 2579 | 1.00 | 1.00 | 137 | 0.94 | 0.93 |
| splash2-lu-n | - | 15167 | 1.27 | 1.27 | 465 | 0.93 | 0.89 |

**Table 4.4: Application Performance and Energy –** Speedups and normalized energy ($E_{norm}$) are all relative to SFVR. All applications are instrumented with activity hints. Some do not report progress hints. **Architecture results thanks to Christopher Torng*

efit from providing a 10x faster response to varying voltage levels. Note that the extra power during a transition comes from the fact that a core needs to be at a slowest clock while supply voltage either increases or decreases above the minimum level mandated by the DVFS plan.

The above system results suggest that RPDN can meet the demands set forth by the study in Section 1.2.2 and can provide the predicted gains for multi- and single-threaded applications for the target eight-core system. Thus, further investigation of RPDN as an enabler for fine-grain voltage scaling is promising direction, that will be pursued in the remaining chapters.

# Chapter 5

# RPDN Design

Having obtained promising system-level results for RPDN, in this and subsequent chapter we proceed with the design and physical implementation of an RPDN circuit. Additional trade-offs and impact of particular circuit design details need to be considered for a successful physical implementation of RPDN. In this chapter, we consider the SC converter design trade-offs in the context of RPDN and then move on to RPDN specific components. Ultimately, the goal is to validate the RPDN concept and assertions sketched out in the previous chapter against real circuit design challenges.

## 5.1 Switch to Capacitor Area Design

Before exploring design of RPDN based on SC, it is important to understand the design tradeoffs associated with SC converters in general. This topic has been extensively studied in [43]. Previous works often assume that total area is a fixed parameter dictated by the application constraints [29] and only one load is considered. For the purposes of RPDN, the concept of area becomes a variable i.e. capacitors can be reassigned between loads. However, the size of

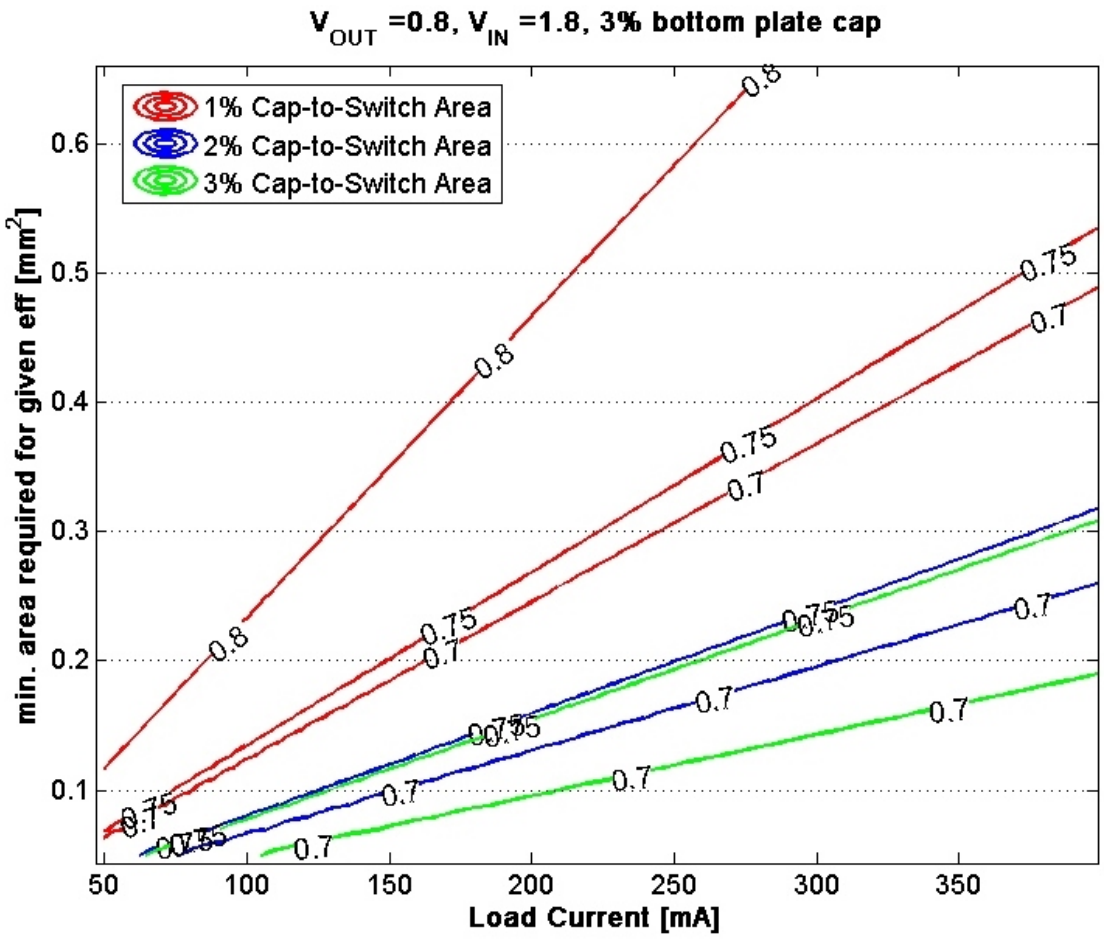


**Figure 5.1: Min capacitance required to achieve efficiency at a given current –** is a strong function of switch area. In genreal for Sc converters, bigger switches result in less capacitance required for given current but also limit peak efficiency that can be acheived. For example designs with 2% and 3% switch-to-capacitance area can never achieve 80% efficiency

the switches for a SC converter remains a key design parameter that requires further consideration. Figure 5.1 shows minimum capacitor area that will be required to achieve certain efficiency for increasing current at 0.8V output in 2:1 configuration in 65nm technology using MOSCAPs. Note that the capacitors dominate the total area of four switches required to realize a 2:1 converter. If designing for minimum area, peak efficiency is reduced; if designing for peak efficiency a very large area is required especially at higher currents.

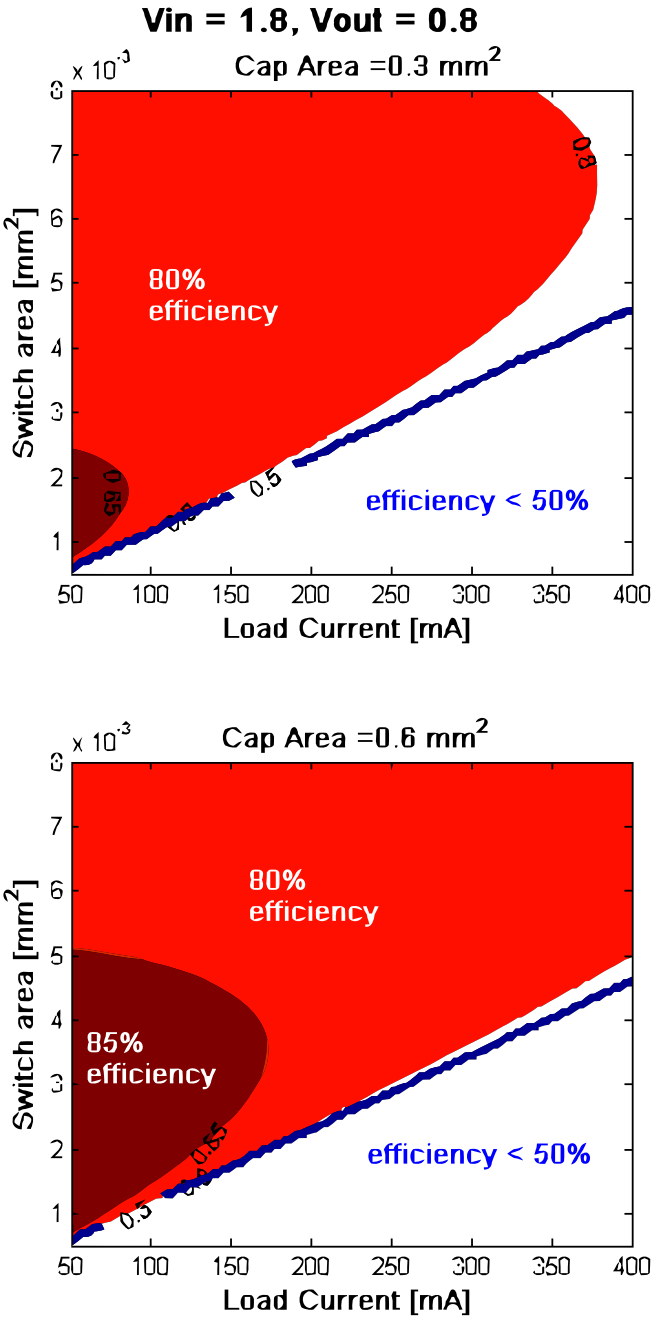


**Figure 5.2: Switch Area vs Load Current Efficiency Contours –** For RPDN its best to add switch area proportionally with capactiance to stay on the peak efficiency area.

Typical designs target a narrow range of current operation and as such a fixed switch-to-capacitance area ratio is sufficient. However, if the desired current range is large and area is limited, then a variable switch size might be an interesting option for area constrained designs that do not frequently operate at high currents due the resulting reduced efficiency in that range. This approach is can be visualized by moving along a horizontal line in Figure 5.1. Such an optimization approach is orthogonal and complementary to RPDN. For RPDN we choose a fixed switch-to-capacitance ratio to avoid complexities in subsequent design procedure. This is equivalent to moving along the contour lines. Combining fixed RPDN approach and variable switch size optimization approach would result in movement in between the lines and horizontal line as the load current varies. Figure 5.2 illustrates the RPDN switch optimization approach in another dimension on a contour plot for two different capacitor sizes. Note the dark red 85% efficiency region is extended for the larger area. At this point it is important to point out a 'cliff' where efficiency falls off dramatically to less then 50%. This needs to be taken in to account and certain amount of overprovisioning is necessary. A design that lies on the edge, while having minimum area can easily fail in presence of process variation or unaccounted series resistance.

## 5.2 RPDN Capacitance Allocation

One benefit of a fixed switch area is that it makes it easier to treat RPDN as unit capacitance cells, that be reallocated to a particular load. Each unit capacitance cell's switch area is fixed. In this way as capacitance is added to support a higher load current, so is a proportional switch area. Unit capacitance cells are discrete and can only be reallocated incrementally. Thus, two questions emerge: 1) what

is the optimal capacitance allocation given a number of loads with different operating points? 2) how many unit capacitance cells are needed to approximate an optimal allocation. To answer the first question, system efficiency can be defined as

$$\eta_{system} = \frac{\sum_{i=1}^{i=cores} V_i I_i}{V_{chip} I_{chip}} \tag{5.1}$$

Thus, for every load condition, there exists one or more optimal allocations, which maximizes $\eta_{system}$. It can found by setting the number of divisions to a high number and then simply searching for configuration with the higest $\eta_{system}$. Note that for $C$ cores and $DIV$ divisions, the number of possible allocations is given by:

$$\textbf{No. of Allocations} = \binom{C + DIV - 1}{C - 1} = \frac{C(C+1)...(C+DIV-1)}{(DIV-1)!} \tag{5.2}$$

A Matlab script was written to automate the procedure. After finding the best allocation, the number of divisions was reduced until $\eta_{system}$ was 0.5% less than $\eta_{system}$ with the optimal allocation. It was found that 20 divisions for 4 loads is in fact sufficient. While this procedure is straightforward in Matlab, circuit implementation should be considered at this point. Table 5.1 shows that the number of allocations as calculated by Equation 5.2 grows very fast with the number of cores and divisions. Hardware would need to be implemented that can make the decision on the order of up to 10s of nanoseconds. Such fast decision could be only made if a simple look up table is hard coded, but that is only possible if the number of allocations is small. More complicated RPDN would require convex optimization algorithm to arrive at the optimal allocation given a particular loading condition.

| Number of Divisions | Number of Cores | Possible Alloctaions |
|---|---|---|
| 16 | 4 | 969 |
| 20 | 4 | 1771 |
| 30 | 4 | 5456 |
| 16 | 8 | 245157 |
| 20 | 8 | 888030 |
| 30 | 8 | 10295472 |

**Table 5.1: Number of possible RPDN unit cell allocations as a function of number of cores and divisions**

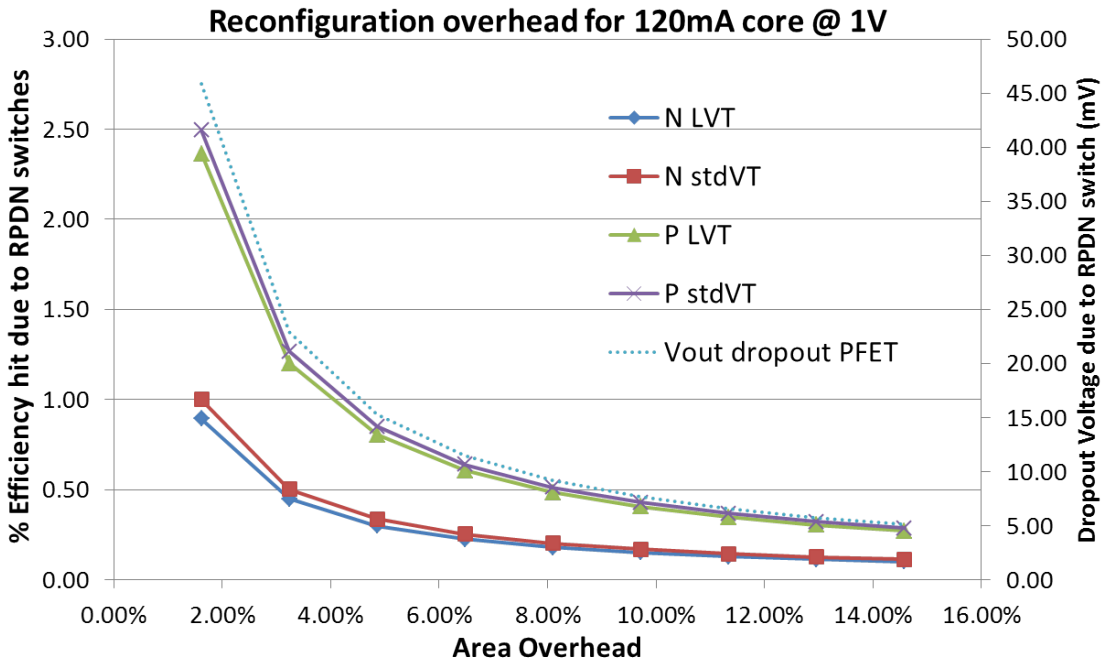


**Figure 5.3: RPDN Switch Overhead –** Bigger power switches have less loss but also add more the RPDN area overhead. The Small dropout voltage caused by the switch can be easily compensated by supplying a higher input voltage to the converter.

## 5.3 RPDN Power Switch Tradeoffs

Following preceding discussion, a structure now for RPDN now emerges that is similar like that of Figure 4.8. Each unit cell is designed independently and consists of eight phases to reduce ripple at the output. The final addition to

make RPDN possible is the switch fabric i.e. the power switches that reassign the unit cells' outputs to a particular load. These switches should be made large as they switch infrequently and the gate are insignificant. Due the finite resistance of the switches, they add a small amount of voltage drop at the output, however, this could be easily compensated for by increasing the supply to the converter by the equivalent amount. Nevertheless, the power switch resistance directly impacts the efficiency through resistive loss; alternatively making the switch larger increases the area overhead of the RPDN. This trade-off is illustrated in Figure 5.3 by using 1V breakdown devices from 65nm process. As expected, best results are obtained with NFETs, but the drive strategy is significantly more complicated compared to the PMOS switch as will be discussed in more detail in Section 6.3.1. For now, it is sufficient to observe that the power switches degrade the efficiency by less then 1% with at most 4% additional area for a 4-core RPDN.

## 5.4 Transient Response

As mentioned in Section 1.2.2, short voltage transition time is of paramount importance for modern multi threaded workloads. Voltage regulators typically employ a feedback loop to guarantee a fixed output voltage for a changing load current. The dynamics of the loop must be chosen to prevent instabilities or secondary oscillations while at the same time producing fast response. These are conflicting requirements that need to be properly balanced. Various control strategies have been proposed in literature. The most conventional one is a frequency based loop based on a charge pump and voltage controlled oscillator (VCO) [28]. Others use a flip-flop based hysteretic control which combines frequency and duty cycle control to help with transient events [19, 20]. Another

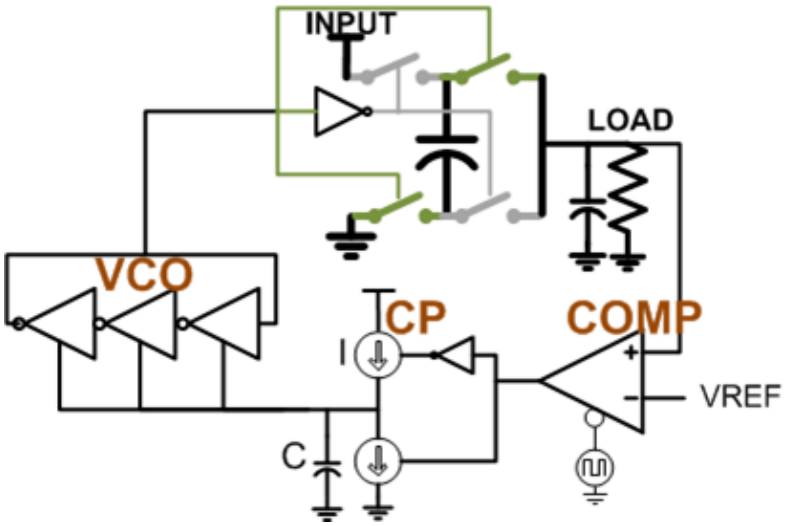


**Figure 5.4: Standard Frequency Control Loop –**

approach is to use fixed frequency and vary the amount of capacitance to accomplish regulation [40]. Finally, a third attempt at combining the two methods is presented in [48] mainly for ripple reduction at low loads. In this work, a standard frequency loop with a charged pump and its integration with RPDN is explored. RPDN helps to improve the dynamics for the loop by effectively augmenting the control with capacitance modulation. However, other control approaches as referenced above could also be integrated with RPDN.

### 5.4.1 Control Loop

A frequency compensation loop is considered as illustrated in Figure 5.4. Output voltage is sensed by the comparator which generates up-down pulses for the charge pump which acts as and effective integrator. The output of the charge pump controls the VCO. The output of the VCO is then divided down into number of phases phases required. Alternatively a slower, multistage VCO can be used to generate all the required phases. Further description of the clocking implementation can be found in Section 6.2.3. The dynamics of the loop are de-

termined by comparator clock, ratio of the charge pump current and capacitor and the vco gain. For a given comparator clock the dynamics are expressed by:

$$f_{vco} = f_{min} + Kf_{min}(\int_0^t \frac{I}{C} sign(V_{out} - V_{ref})dt \tag{5.3}$$

Equation 5.3 indicates that higher $I/C$ ratio provides faster response time and thus better output voltage tracking of $V_{ref}$ by the regulator. On the other hand, setting $I/C$ too high leads to output oscillation as the regulator alternately over and under compensates. This output oscillation adds to an already existing ripple at the output due to fundamental operation of the converter. It is most problematic in the light load condition and when target output $V_{ref}$ is significantly below ideal voltage for a given conversion ratio. Assuming the output voltage is relatively constant and sampled by the comparator with clock frequency $f_{comparator}$, the output voltage oscillates with $f_{comparator}$.

### 5.4.2 Determining the Transient Settling Time

For the purposes of estimating the transient response of configurations in chapter 4 and choosing the correct parameters for the frequency loop, one can start the design process by placing a limit on the output oscillations at light load to 10% of the DC output voltage. For a particular converter and VCO design, a predetermined $f_{comparator}$ and load current and voltage extremes, this sets a limit to highest allowable $I/C$ ratio. Once this is known, the regulator's response time can be easily established thanks to a direct mapping that exists between converter frequency and the output power it can provide. An example of such mapping is shown in Figure 5.5 for RPDN and MAVR. As output voltage increases, so does the load current according to DVFS plan as described in Section 4.1.2. This is another advantage of designing for a specific load. For the target

system, described in Section 4.1.1, the power consumption for typical loads is known based on architecture level simulations, it varies only with in 10% for a fully active core. (For more complicated out-of-order cores, there is potential for complex load behavior, for example when there is a stall due memory miss followed by intense period of computation). Key observation from the plot is that converter frequency is an exponential function of output power. What this means is the output voltage is very sensitive to a change in converter frequency when power is low. Likewise it is very insensitive to converter frequency when power is high. Note, that typical VCO's frequency dependence on control voltage is linear; similarly the charge pump output voltage changes linearly with current. Further modification for this control scheme will be discussed in Section 6.2.2.

The 10x improvement in response for RPDN over MAVR comes about in two ways: First, most transitions in RPDN covers a narrow frequency range because unit capacitance cells are added and subtracted as the output power is varied as indicated by the black solid line. Second and more important effect has to do with $I/C$ ratio choice. For MAVR, a converter sized for the maximum power (area > 0.18mm$^2$) requires a low value for $I/C$ to limit oscillation for $P_{out}$ less than 10mW. For RPDN the converter area is reduced to 0.03mm$^2$and the resulting converter has little effect on the output power provided to the load. This translates to a smaller output voltage oscillation for the same frequency variation due under and over compensating by the charge pump. Thus, $I/C$ can be set about an order of magnitude higher relative to MAVR. The estimated response are summarized in Table 4.3.

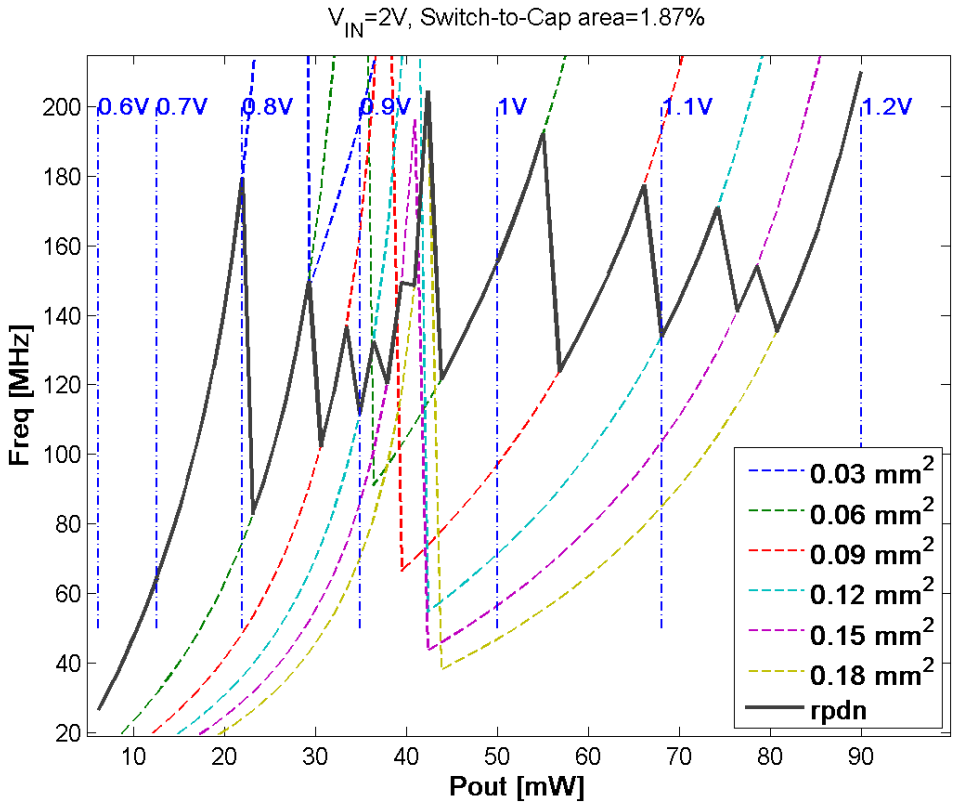


**Figure 5.5: Converter Frequency vs Output Power for Different Capacitor Size** – SC converter's output power has an exponential dependence on switching frequency. To cover a wide load range MAVR (0.18 $mm^2$ or more) has to cover a wide range frequencies, resulting in slow performance at high power As power and voltage of the load increase, RPDN adjusts the converter size, keeping the frequency in a narrow range (black line). *Here, the MAVR and RPDN designs are twice the area of designs in chapter 4 to support higher power*

## 5.5 RPDN Area Savings

In this section we analyze the impact of RPDN on the area and efficiecny overhead. First, we look at system level efficiency and area impact. For this purpose we consider a four-core RPDN with 20 unit cells. As discussed in the next chapter, certain implementation overheads such as clock SC clock distribution or power routing may make an eight-core RPDN challenging to design. However, an eight-core RPDN could be partitioned to 2 four-core RPDNs. Figure

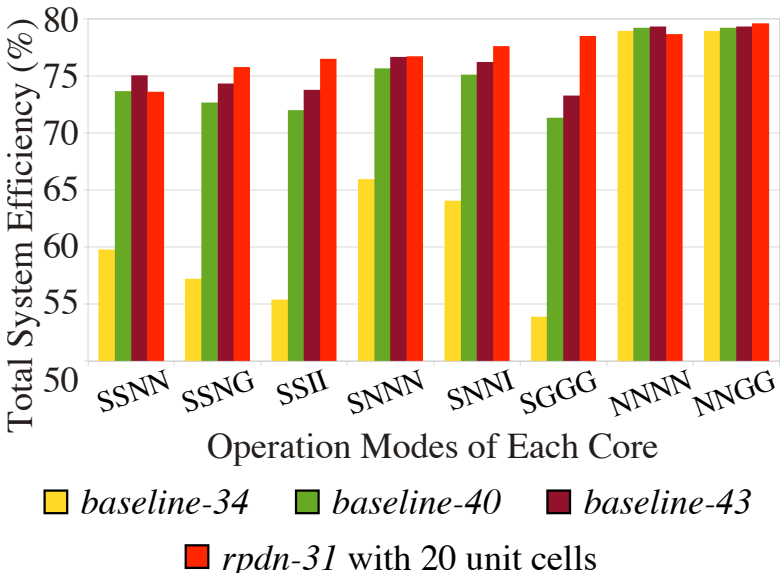


**Figure 5.6: Estimated System Efficiency for Various Configurations –** *baseline-34*, *basline-40*, *baseline-43*, *rpdn-31* use 0.34, 0.40, 0.43, and 0.31 $mm^2$ respectively; G = gated mode w/ 0V@0mA; I = idle mode w/ 0.6V@10mA; N = nominal mode w/ 0.8V@50mA; S = sprinting mode w/ 1.1V@80mA; results for 65 nm CMOS using steady-state analytical model of just voltage regulators.

5.6 shows system efficiency (Equation 5.1) for various core operating mode configurations. For this loading scenario, a much smaller RPDN design compares favorably to a MAVR design that takes 40% more area. The actual area savings for RPDN depend on specific operating modes and the different power values between the modes. In general, the less simultaneous sprinting cores need to be supported and the bigger the power difference between sprint and idle, the larger the area savings that RPDN can provide. The estimate in Figure 5.6 is a conservative choice since there is about 2x difference in power from 0.8V to 1.1V. The power difference comes down to the choice of frequencies at which the cores operate for a given supply voltage. According circuit simulations from Section 4.1.2, the maximum frequency increase that could be obtained between 0.8 and 1.1V would result in a 3x operating power difference. Note that the 40%

estimate does not include the RPDN power mux switches which can diminish the area savings from 3% to 10% of depending on implementation details.

In chapter 4 we started with a Matlab level description of voltage regulators to arrive at the RPDN concept. This model was then refined to include leakage for low power levels and transient response estimation. This was followed by a spice-level circuit model that confirmed the accuracy of the Matlab predictions for efficiency and area estimates. However, the control loop is a verilog-A model of the various blocks that would have to be implemented in a real circuit. The final step is designing a functional RPDN circuit that only contains transistors and includes the parasitics of the interconnect along with test circuits to measure the fabricated circuit. Detailed circuit-level implementation of RPDN explored in the next chapter.

# Chapter 6

# RPDN Circuit Implementation

Structured, hierarchical approach is key to implementing RPDN. The circuit involves additional complexities that are not present in a single load DC-DC converter design. For example, there are four independent control loops, one for each load. Each loop generates its own clock domain; then each clock domain has 8 phases, resulting in 32 clock signals that must be routed to every cell on chip. Control signals for cell allocation must also be preprogrammed and stored in address registers that can flipped to alternate configuration in a matter of nanoseconds. Supply and load power plane routing becomes more challenging, which necessitates careful floor planning for the required individual switched capacitor cells at each hierarchy level. The design of a highly hierarchical structure for tractable design will be described in this chapter. Further refinements of the RPDN circuit concept are considered as interesting implementation details emerge.

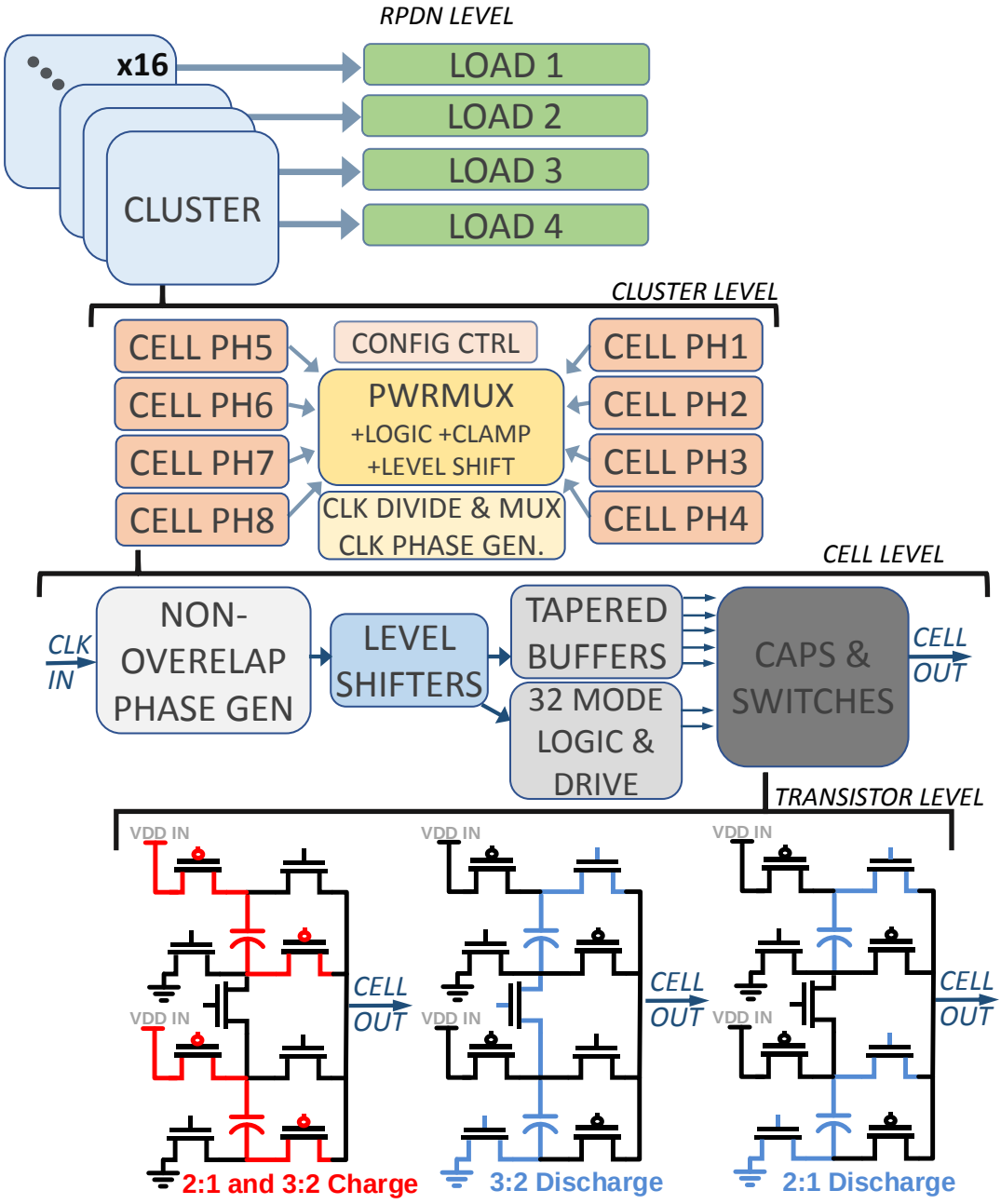


**Figure 6.1:** RPDN Hierarchy

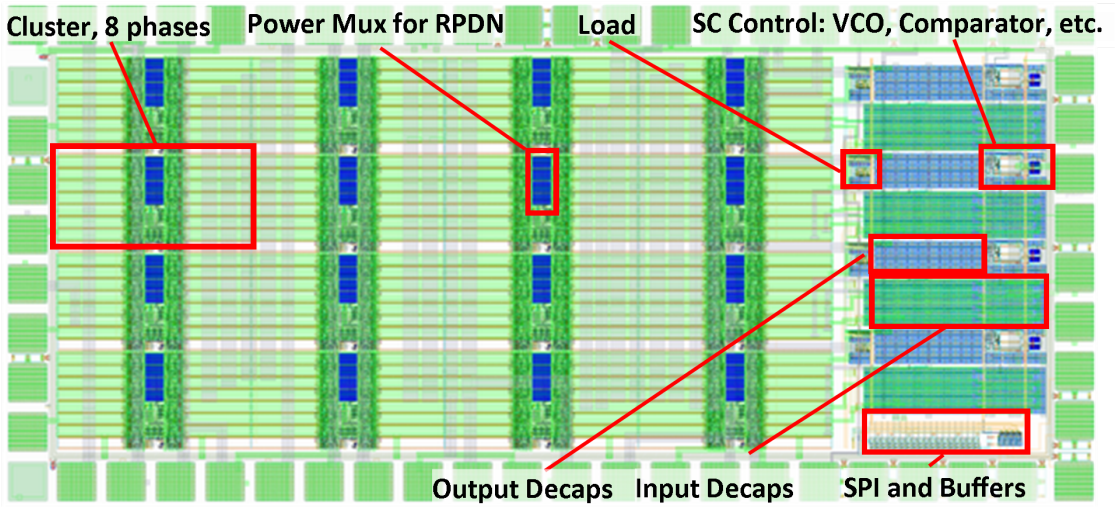


**Figure 6.2:** Full RPDN Chip Layout

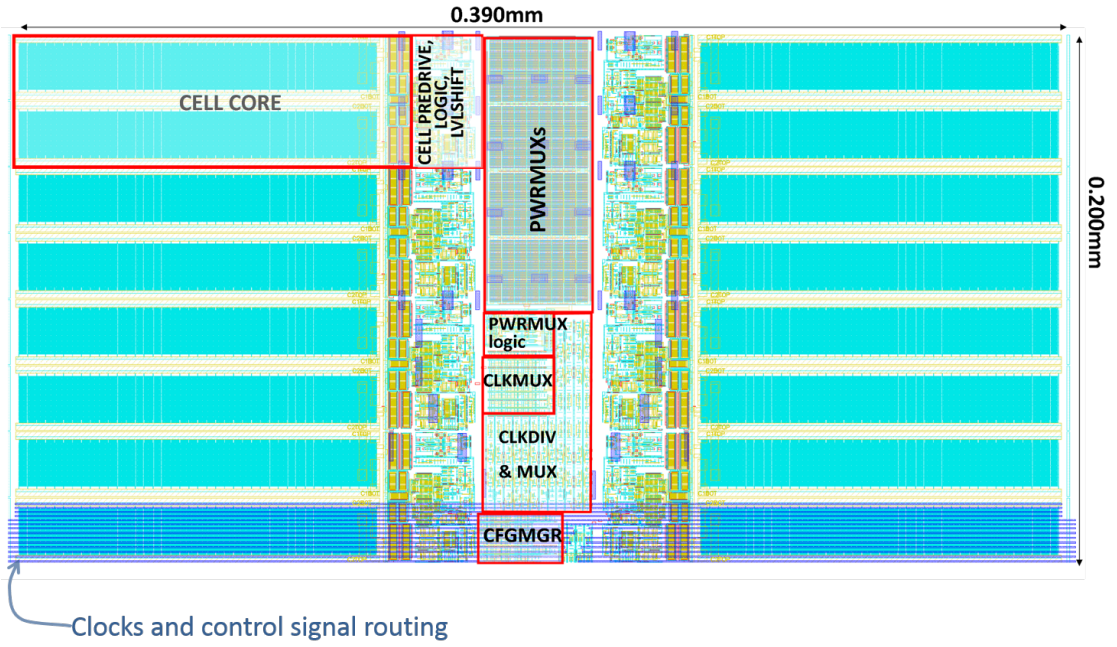


**Figure 6.3:** Cluster Floorplan

## 6.1 Cluster and Cell Hierarchy

The RPDN design implementation is started by partitioning the circuits into hierarchy as seen in Figure 6.1. For a 4-core RPDN circuit, from previous section, at least 16 clusters are required. Each of the clusters is independent and can channel its output to one of the four loads. A cluster is defined as a conglomeration of 8 cells each operating with a phase of the clock offset by 45 degrees. Therefore each cluster receives four clocks from the control loops and multiplexes between them depending on which load is the cluster allocated to. Clock routing and phase generation are described in more detail in in Section 6.2.3. In the initial RPDN model in previous chapter, the power mux switches (more details in Section 6.3.1 were at the cell level. However, additional decode logic, logic level shifter and clamping circuitry that were introduced at this design stage take up area that would unnecessarily have to be repeated in every cell. In general, it is a good strategy to move components up in hierarchy as high as possible to ensure the most compact layout.

Configuration control block holds the registers that determine two states for the cluster. The cluster can switch rapidly between these two states. Each state holds 3 bits: 1 bit to set the 2:1 and 3:2 configuration modes for all the cells in the cluster; 2 address bits to set the power mux to any of the four loads. In addition, the configuration control block holds two default states in case the registers cannot be programmed properly.

The cell level takes only two signals as inputs, a single clock and 3:2 mode configuration bit. As such this level is makes up the core of the DC-DC converter that is has no knowledge of RPDN. It is self contained which means it could be further improved locally without impacting RPDN. In fact, most of the

efficiency performance of the converter is determined at this level; only power mux related loss is outside of the realm. The sole clock input is inverted and goes through non-overlap circuit to generate $\phi_1$ and $\phi_2$. $\phi_1$ and $\phi_2$ are cell sub-phases used to alternately charge and discharge the main capacitors as shown on the transistor level in Figure 6.1 The non-overlap circuits guarantees that the switches are turned off before the others are turned on. The choice of the non-overlap duration is chosen to be around 60ps. If this time is chosen too short, additional timing variations due in level shifters and buffers and propagation delay mismatches can cause overlap leading to loss as supply can shorted to ground briefly for example. On the other hand, introducing too long non-overlap duration can also impact efficiency at high operating frequencies as the conduction angle of the switches is reduced, which ultimately limits the maximum power the converter can achieve with good efficiency. The level shifters that follow are similar to the ones in Figure 3.7 and generate high voltage versions of $\phi_1$ and $\phi_2$. Last stage before the power stage consists of tapered buffers, which also include power gating circuits for selected signals depending on the mode of operation. The driving of the mid-transistor and its logic require more consideration. This transistor operates in between 2 and 1V in 3:2 mode and is on during the discharge cycle. But during 2:1 mode it must operate between 0 and 1V to prevent oxide breakdown, while keeping the device in the off state. In fact, it is needs to be clamped to either the output of the cell rather then a fixed 1V supply. A different, more complicated approach was taken to accomplish this task compared to [29] which uses a floating inverter. Figure 6.4 shows the schematic of the final driver stage. The driver utilizes only 1V devices and offers a significant speed advantage so that the drive signal for the mid transistor stays within the timing budget.

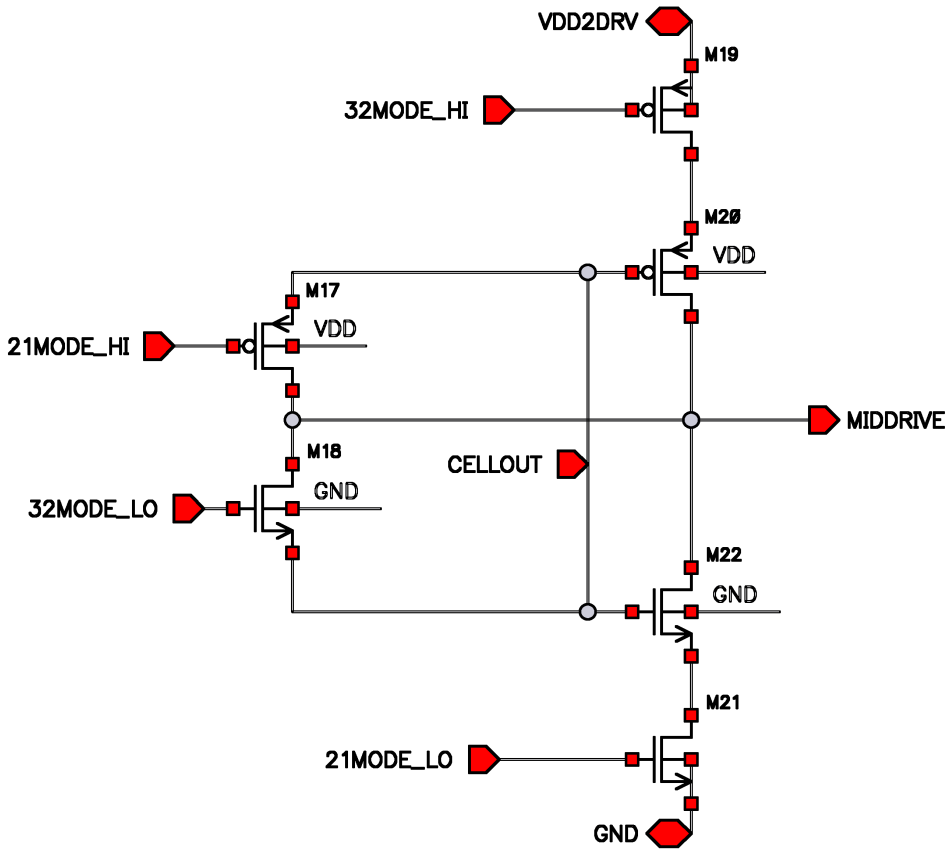


**Figure 6.4:** Mid Transistor Driver Design

The operation of the circuit is such that transistors M18 and M19 are switched in 3:2 mode, causing middrive signal to go between CELLOUT and VDD2DRV. In 2:1 mode M21 and M17 are switched and the drive signal is between CELLOUT and GND. Transistors M28 M22 only serve to prevent over voltage stress on M21 and M19. All switches are driven independently with specialized logic that includes high voltage transmission gates and pull up/down transistors to turn off the unused devices. Finally, the power stage level is similar architecture to [29] but simplified to not include the 3:1 mode. During initial design phase using the analytical Matlab model, it was found that the 3:1 mode has little efficiency benefit for the voltage ranges of the target system compared

to regulating down a 2:1 mode to 0.6V. At the same time the 3:1 mode adds significant complications to power stage and cell design. The ratio of switch to area was chosen at 4.2%, which is higher then 3% considered in previous chapter to account for additional parasitic resistance of traces.

Overall, the addition of the power stage drivers and the mid-transistor drive scheme degrades the efficiency by about 1-2% from the Matlab model prediction in previous chapter. This to be expected as those circuits are not accounted for in the model. Exact power optimization of these stage could push this number down to 1%. The drivers were over-designed for two reasons. First to allow flexible choice for a power stage and potentially accommodate bigger power switches, if it was found necessary later in the design process. Second, to make the design robust against process variation and anticipate parasitic capacitance and resistance due to wiring that would inevitably be added during layout stage. The loss due to the driver circuits becomes much more pronounced at low current levels (< 10mA) where it becomes a greater part of total power delivered to the load. In fact, yet another benefit of RPDN is scaling this loss by adjusting the size of the converter dynamically based on load demands. This is a similar technique employed in buck converters [26] and [46].

## 6.2 Realistic Control Loop

The control loop in the physical implementation underwent significant changes from the one presented in Figure 5.4. The changes necessary for functional implementation will be described in this section.

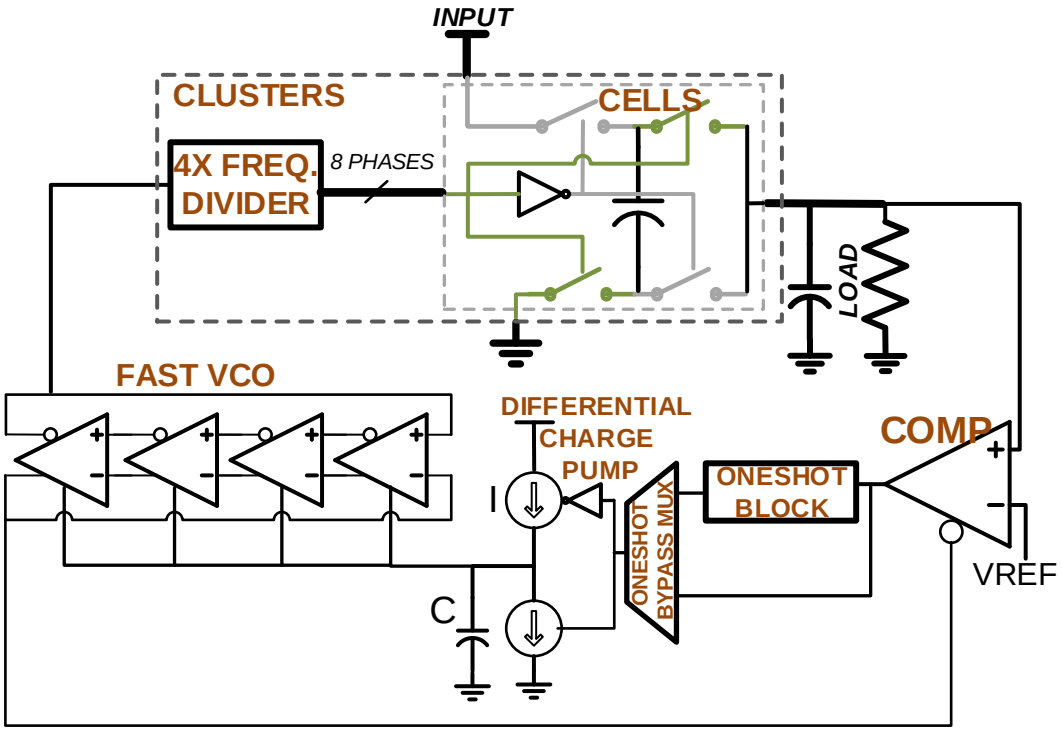


**Figure 6.5:** Implemented Control Loop for RPDN

### 6.2.1 Comparator Clocking

In previous chapter, a separate 100MHz clock was assumed for the comparator for the transient time simulation. The reasoning was that the faster clock limits the maximum ripple at the charge pump output $V_{ctrl}$ and thus reduces the frequency variation of the converter minimizing the secondary output voltage ripple as discussed in Section 5.4.2 when converter switching frequency is low. On can imagine that an even faster comparator clock might be even more beneficial and a 1GHz clock was used to test this theory in simulation. Aside from the fact that this solution would require a separate oscillator, this solution means that the output is effectively sampled asynchronously. Recall that the output ripple is synchronous with the main VCO clock. In the limit where the comparator clock is much faster then the ripple, the output is sampled continuously. But

that assumption is not entirely correct as the fundamental frequency of the output ripple is the converter frequency multiplied by the number of phases. In the worst case, the sampling frequency can form an unpredictable beating pattern with the output ripple due to the asynchronous relation between the two. In fact, the beating pattern only appeared on one of the corners, making it difficult to predict or find the worst case secondary oscillation, and what follows, to properly design the converter's feedback loop for best possible response.

A better solution is to use the converter's VCO to clock the comparator. Then the output voltage is always sampled at the same point relative to the ripple frequency. For reasons described in Section 6.2.3 the VCO is running at 4x the frequency of the converter, or half the fundamental frequency of the ripple. This ensures a faster response to a change in output voltage than if the VCO was running at converter's frequency. This approach results in a predictable behavior of the secondary oscillation that can be reduced by trading off response time.

### 6.2.2 One Shot vs Linear Charge Pump Current Control

In the previous chapter, linear charge pump current control was considered, meaning the charge pump always pulls the VCO to either run slower or faster; it cannot maintain the frequency. This is similar to a bang-bang phase detector. From the converter point of view, it means that the output is always either too high or too low resulting in small oscillation around the target voltage (on top of the converter ripple). Another conclusion from previous chapter was that converter has an exponential dependence on output power as seen in Figure 5.5. As a result, the converter's regulation of the output voltage is to sensitive to changes in frequency at low power and not sensitive enough at high power. One way to mitigate this effect is to use a one shot block following the comparator.

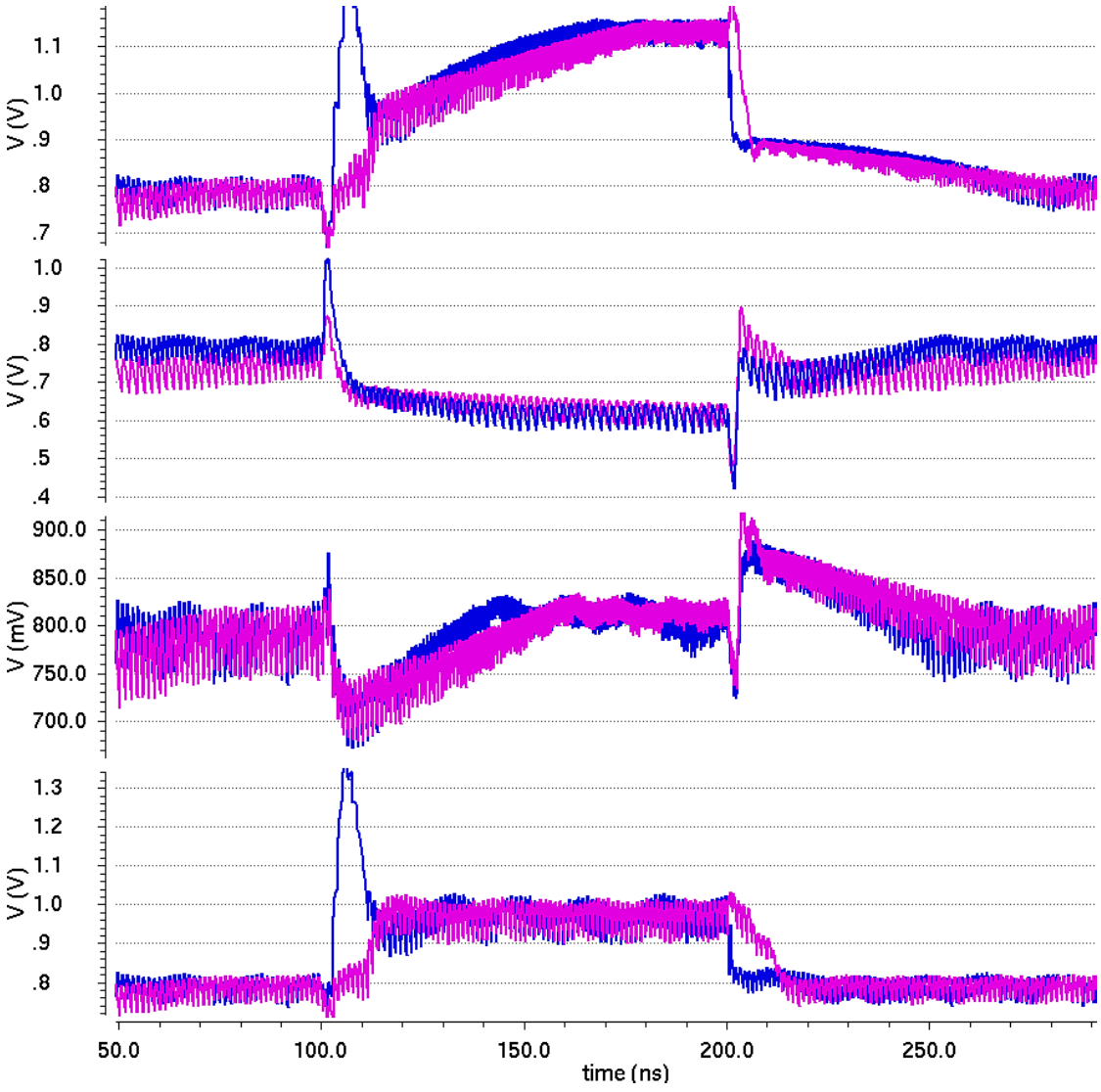


**Figure 6.6:** Transient Response of the Implemented RPDN Circuit – 4 loads and 16 clusters are reconfigured to various voltages at time=100ns and then back to the original configuration at time=200ns. Blue represents linear charge pump control and purple is using oneshot.

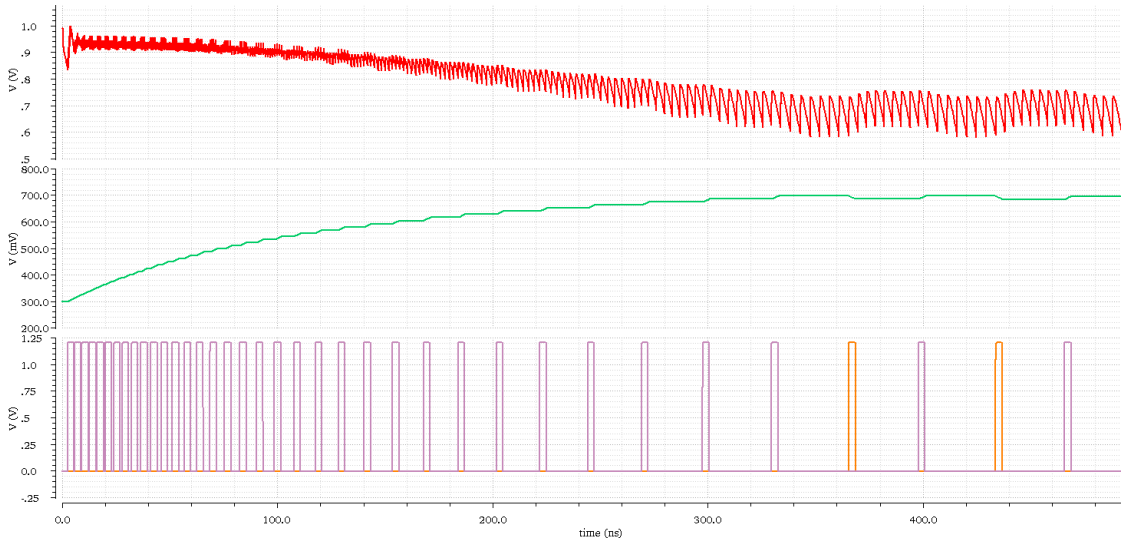


**Figure 6.7:** Transient Simulation Using Oneshot in Feedback Loop – Rate of pulses that control the charge pump and update $V_{ctrl}$ is proportional to the frequency of the converter. Orange pulse is speeds up the VCO, purple slows it down.Green is the VCO's control voltage and red is the converter's output voltage

Figure 6.7illustrates what happens in the control loop when one shot is used. By forcing the update of $V_{ctrl}$ to be frequency dependent, the one shot block causes the control loop to have a complementary response to converter's output power dependence on frequency as illustrated by the green curve in Figure 6.7. This is in contrast to a linear charge pump control where to curve only follows a linear trajectory. A dynamic reallocation of a core RPDN is shown in Figure 6.6 for the same loading cases with and without the use of one-shot. The charge pump current was increased by eight times to ensure a similar response time for a fair comparison between the two. The one-shot shows slightly less secondary ripple once steady state, but it is not clear which method is better and further investigation is necessary, which is why both schemes are implemented on chip. The linear control has relatively faster response at low switching frequency but slower at fast switching frequency, so the choice of charge pump current is different then for the one-shot. One could optimize for the same sec-

ondary oscillation magnitude or for the same response across a range of voltages and the conclusion would be different for each case. Further extensions and improvements to this scheme is discussed in Section 7.1.

### 6.2.3 VCO and Clock Distribution

While a single ended VCO was adequate for first order modeling of the control loop, a real circuit will have significant supply noise that can affect the VCO's frequency. It is well known that single ended ring oscillator based VCO's are very susceptible to supply and ground noise. Jitter and phase noise are secondary considerations in this application and they should not have significant impact on the output. Still a fully differential VCO offers much better supply noise immunity. Additional benefit is that it can have an even number of stages and so 8 phases can be tapped out very easily. Although the VCO can readily provide 8 phases, recall that for the RPDN circuit, there are 4 loads, each with its own VCO. This means 32 clocks would have to routed properly across the whole chip. An alternative solution chosen in this design is to route 4 faster clocks. Each one can be locally divided using a standard frequency divider consisting of 4 flip flops in a loop configuration thus producing the required 8 phases.

## 6.3 Reconfiguration Dynamics

The discussion in previous section is equally valid for single load switched capacitor converters as to RPDN. In this section additional considerations specific to RPDN are examined such as the power mux design, clock reassignment and mode selection during reconfiguration and testing of RPDN circuits.

### 6.3.1 Power Mux Design

The key challenge in the power mux design is minimizing the series resistance, which can impact efficiency overheads of RPDN as shown in Figure 5.3. The RPDN implementation was done in a low power version of the 65nm process, where the switches are optimized for low leakage at the expense of increased series resistance. For this reason, thin oxide, low Vt NMOS was used for power mux for better performance to area ratio.The target output voltage range is 0.6V to 1.2V, so 0V is required to completely turnoff the NMOS in case some of the loads are powered down to 0V. On the other hand, 2V is necessary to fully turn on the NMOS when conducting. However, at the instant of powering up a load, which can be close to 0V, setting the gate of an 1.2V rated NMOS to 2V can cause voltage stress at the oxide. Thus a clamp in feedback configuration is employed as shown in a simplified schematic in Figure 6.8. Each power NMOS has the same circuit wrapped around it (not shown in the circuit diagram). If the LOAD3 is at 0V, the inverter turns on the clamp, which sinks current from the thick oxide predriver, such that the gate voltage does not exceed 1.4V. The size of the clamp is chosen carefully for this case and the inverter also has a low transition voltage to ensure the clamp turns off promptly. The level shifter is a regenerative one as shown in Figure 3.8. The thick oxide drivers are purposefully under-powered for a few nanosecond transition as the power mux does not need to switch too fast.

### 6.3.2 Cluster Clock and Mode Selection for Reallocation

The power mux is responsible for reassigning the output of the cluster to a desired load. But the input, namely the clock frequency needs to be matched to a

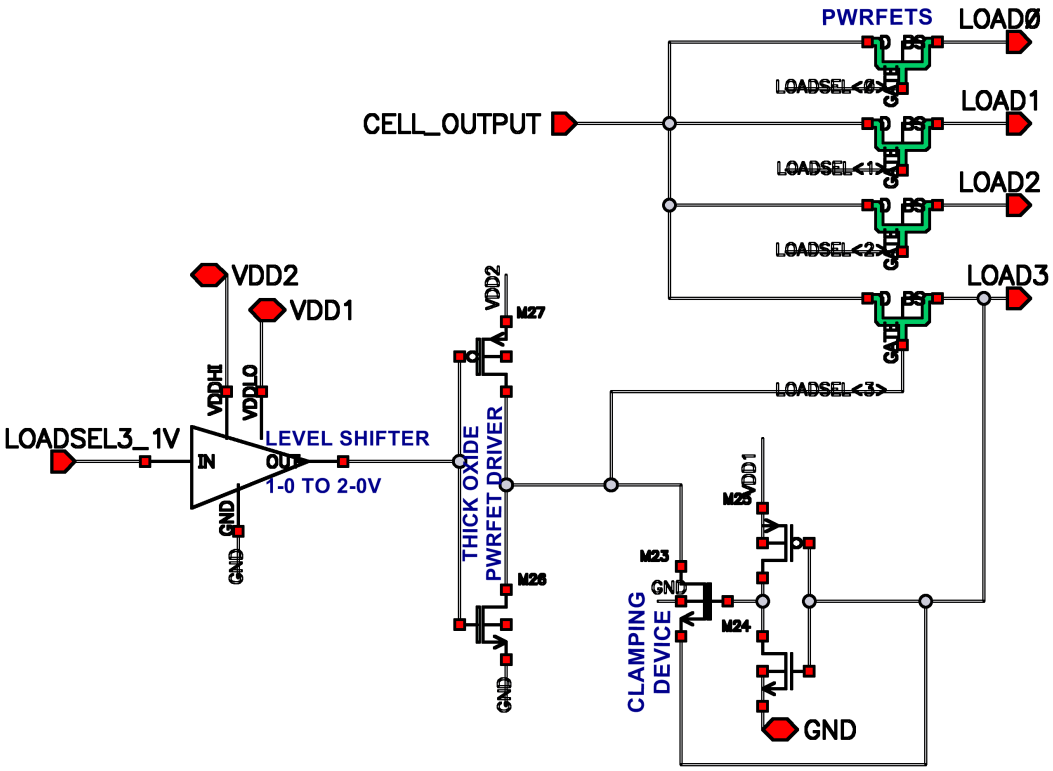


**Figure 6.8:** Power Mux Clamping Circuit

corresponding control loop that regulates the voltage on the desired load. This is accomplished with eight 4-to-1 clock muxes that are positioned after the clock divider in the cluster. Thus each clock domain requires its own set of 4 flip flops for frequency division. A better solution might be to mux the four clocks and then divide afterwards, thereby saving area and power by only requiring one clock divider as opposed to four. The reason for that lies in the details of the clock divider. Flip-flop based 4x clock divider needs to be initialized to a correct state for proper operation. If a sudden jump to a new random frequency occurs, it is possible that the divider goes into one of those undesired states, lest some special circuitry is designed to prevent such a case.

The power mux and clock reassignment occur almost instantaneously once

the control signal is received from the configuration manager. For most voltage transitions, this results in a relatively well behaved response. However, a few transitions as shown by the blue curve on Figure 6.6 show a large peak even up to 1.3V, which is above the voltage rating of the process. This peak is related to cells abruptly switching from 2:1 to 3:2 mode. In 2:1 mode, both capacitors in the operate in parallel and have $V_{dd}/2$ voltage across them on average. Switching to 3:2 mode, mid-transistor is activated as shown in discharge diagram in Figure 6.1 stacking the two capacitors. This leads to an abrupt increase in the output voltage. A solution to smooth out the transition is to stagger each phase such that the mode control signal occurs sequentially for each phase as opposed to all phases at once. This allows each phase to gradually balance the charge on the capacitors to the new value $V_{dd}/3$ as required in the 3:2 mode. This can be accomplished by gating the mode control signal at the cell level with the cell clock using a flip flop. The technique was successfully tested in simulation and triggering on the positive, negative or both edges of the cell clock were all tested. The positive edge generally gave the best results. The improvement using this scheme is readily visible in reffig-hier-diagram by comparing the purple curves which include the flip flop gating circuit for each phase.

# Chapter 7

# Conclusion

This work investigates various on-chip power delivery schemes for dynamic digital loads. First, a single load that is powered with an inductor based converter is considered. The proof of concept, 3-level buck converter was designed and fabricated in 65nm CMOS technology, and the measurements showed reasonable agreement with predicted performance improvement at light loads using quasi-resonant switching scheme. The 3-level converter combines the advantages of both switched capacitor and inductor based topologies and has many advantages in fully integrated solutions. However, it also has limitations as it is difficult to scale down for smaller loads. Specifically, a system consisting of 8 in-order cores with local caches was considered as a target load. A 3-level converter would be well suited to power four or more cores together, but not each core individually. Yet, high level system studies with real multi and single threaded workloads show that there is potential for significant performance improvement if dynamic, per-core voltage regulation can be accomplished fast enough. Various organizations of voltage domains were considered as the design space of switched capacitor converters was explored. In the end, RPDN was proposed and studied in more detail as a way to mitigate area overheads,

improve efficiency at light load and finally improve the response time of the of the regulator. First, a conceptual model using Matlab was developed, followed by a high-level, but realistic transistor and Verlog-A circuit model. This was followed by a physical implementation of RPDN. At each step, the concept was refined further and new, interesting circuit level solutions were explored.

Fully-integrated, switch mode power supplies are becoming an active research topic, especially with recent developments in passive device technology integration. Applications of such supplies are not limited to microprocessors. There is considerable interest for various radio frequency applications or power harvesting systems, to name a few, where integrated solutions benefit from a targeted design of the converter for the particular demands of the load. In addition, the co-design of the load and power supply leads to an exciting new opportunities in the system level optimization that were not possible before; RPDN is one such example.

## 7.1 Future Work

One of the most fundamental questions that emerges is at which point is an inductive based converter better or worse than a capacitative converter? The answer to this question largely depends on application. For battery operated or energy harvesting systems the most important metric might be steady state efficiency. For precision analog and RF circuits, low ripple might be most important factor. For dynamic loads, as outlined in this work, fast response and area efficiency might be the most important metric. There have been a few attempts in literature to provide figure of merit for various switch mode power supplies [42, 44, 51], but they only consider a few aspects of the converter men-

tioned above. An all encompassing figure of merit similar to LNAs and PLLs could help distinguish and rate devices for best application. This is especially true considering the emergence of deep trench capacitors and magnetic materials in integrated converters.

As is usually the case, in actual physical design procedure, the RPDN implementation sheds light on certain nuances that may not have been apparent at first glance. Some of those were mentioned in chapter 6, but some other promising improvements are listed below. (1) Schedule a dynamic increase in charge pump current during reconfiguration. Presumably an external control schedules the dynamic voltage levels for each load. As such, an instance of change of the voltage is known and this information can be easily passed to the converter to temporarily boost the charge pump current for faster convergence to a new value. In [28], the charge pump is bypassed to accomplish faster response, but this may be inaccurate and prone to error. (2) Rather then relying on an external controller for voltage, the converter could detect power levels at each load by simply monitoring the frequency of each load and adjust the frequency to stay within some bounds by coarse tuning the capacitance. This would represent a purely hardware approach that would be unable to detect busy-wait periods of the microprocessor. Nevertheless, it could prove very interesting for some systems. (3) Remove the frequency compensation loop altogether and use a frequency/duty cycle control as suggested in [19] for faster response. It remains to be seen if this can easily be integrated with RPDN. (4) Use a hybrid approach where the reconfigurable clusters operated with a constant clock, but preassigned clusters handle regulation by changing their frequency. This would alleviate a somewhat complicated clock routing and division demanded by RPDN. This could be a good approach if RPDNs were to be shared among

many loads, since in its current implementation the clock routing limits scaling of the number of loads that RPDN can support.

# Bibliography


[1] M. Alimadadi, S. Sheikhaei, G. Lemieux, S. Mirabbasi, W. Dunford, and P. Palmer. A Fully Integrated 660 MHz Low-Swing Energy-Recycling DCDC Converter. *IEEE Trans. on Power Electronics (TPEL)*, 24(6):1475–1485, 2009.

[2] G. M. Amdahl. Validity of the Single Processor Approach to Achieving Large Scale Computing Capabilities. *Spring Joint Computer Conference, AFIPS*, pages 483–485, 1967.

[3] T. Andersen, F. Krismer, J. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brandli, P. Buchmann, and P. Francese. A 4.6W/mm2 power density 86% efficiency on-chip switched capacitor DC-DC converter in 32 nm SOI CMOS. *Applied Power Electronics Conf. and Exposition (APEC)*, pages 692–699, 2013.

[4] M. Annavaram, E. Grochowski, and J. Shen. Mitigating Amdahl's Law through EPI Throttling. *Int'l Symp. on Computer Architecture (ISCA)*, Jun 2005.

[5] S. Bandyopadhyay, Y. Ramadass, and A. Chandrakasan. 20uA to 100mA DC-DC converter with 2.8 to 4.2V battery supply for portable applications in 45nm CMOS. pages 386–388, Feb 2011.

[6] T. Burd, T. Pering, A. Stratakos, and R. Brodersen. A Dynamic Voltage Scaled Microprocessor System. *IEEE Journal of Solid-State Circuits (JSSC)*, 35(11):1571–1580, 2000.

[7] B. H. Calhoun and A. Chandrakasan. Ultra-Dynamic Voltage Scaling Using Sub-Threshold Operation and Local Voltage Dithering. *IEEE Journal of Solid-State Circuits (JSSC)*, 41(1):238–245, Jan 2006.

[8] L. Chang, R. K. Montoye, B. L. Ji, A. J. Weger, K. G. Stawiasz, and R. H.

Dennard. A Fully-Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3A/mm$^2$. *Symp. on Very Large-Scale Integration Circuits (VLSIC)*, Jun 2010.

[9] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa. A 0.022mm2 970 uW dual-loop injection-locked PLL with #x2212;243dB FOM using synthesizable all-digital PVT calibration circuits. *Int'l Solid-State Circuits Conf. (ISSCC)*, pages 248–249, 2013.

[10] J. Donald and M. Martonosi. Techniques for Multicore Thermal Management: Classification and New Exploration. *Int'l Symp. on Computer Architecture (ISCA)*, Jun 2006.

[11] R. G. Dreslinski, B. Giridhar, N. Pinckney, D. Blaauw, D. Sylvester, and T. Mudge. Reevaluating Fast Dual-Voltage Power Rail Switching Circuitry. *Workshop on Duplicating, Deconstructing, and Debunking (WDDD)*, Jun 2012.

[12] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge. Near-Threshold Computing: Reclaiming Moore's Law Through Energy-Efficient Integrated Circuits. *Proc. of the IEEE*, 98(2):253–266, Feb 2010.

[13] T. Fischer, J. Desai, B. Doyle, S. Naffziger, and B. Patella. A 90-nm variable frequency clock system for a power-managed itanium architecture processor. *IEEE Journal of Solid-State Circuits (JSSC)*, 41(1):218–228, 2006.

[14] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats. The age of multilevel converters arrives. *Industrial Electronics Magazine, IEEE*, 2(2):28–39, 2008.

[15] V. Gutnik and A. P. Chandrakasan. Embedded Power Supply for Low-Power DSP. *IEEE Trans. on Very Large-Scale Integration Systems (TVLSI)*, 5(4):425–435, Dec 1997.

[16] P. Hazucha, T. Karnik, B. Bloechel, C. Parsons, D. Finan, and S. Borkar. Area-efficient linear regulator with ultra-fast load regulation. *IEEE Journal of Solid-State Circuits (JSSC)*, 40(4):933–940, Apr 2005.

[17] P. Hazucha, G. Schrom, J. Hahn, B. A. Bloechel, P. Hack, G. E. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar. A 233-MHz 80–87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core inductors on Package. *IEEE Journal of Solid-State Circuits (JSSC)*, 40(4):838–845, Apr 2005.

[18] G. Huang, D. Sekar, A. Naeemi, K. Shakeri, and J. Meindl. Compact Physical Models for Power Supply Noise and Chip/Package Co-Design of Gigascale Integration. *Electronic Components and Technology Conf. (ECTC)*, pages 1659–1666, 2007.

[19] R. Jain, B. Geuskens, M. Khellah, S. Kim, J. Kulkarni, J. Tschanz, and V. De. A 0.45um 1V fully integrated reconfigurable switched capacitor step-down DC-DC converter with high density MIM capacitor in 22nm tri-gate CMOS. pages C174–C175, 2013.

[20] R. Jain and S. Sanders. A 200mA switched capacitor voltage regulator on 32nm CMOS and regulation schemes to enable DVFS. pages 1–10, 2011.

[21] D. Kanter. Haswell's FIVR Extends Battery Life. The Microprocessor Report, Jun 2013.

[22] W. Kim, D. Brooks, and G.-Y. Wei. A Fully-Integrated 3-Level DC-DC Converter for Nanosecond-Scale DVFS. *IEEE Journal of Solid-State Circuits (JSSC)*, 47(1):206–219, Jan 2012.

[23] W. Kim, M. Gupta, G.-Y. Wei, and D. Brooks. System level analysis of fast, per-core DVFS using on-chip switching regulators. *Int'l Symp. on High-Performance Computer Architecture (HPCA)*, pages 123–134, Feb 2008.

[24] J. Kimball and P. Krein. Analysis and design of switched capacitor converters. 3:1473–1477 Vol. 3, March 2005.

[25] J. Ko, K. Klues, C. Richter, W. Hofer, B. Kusy, M. Bruenig, T. Schmid, Q. Wang, P. Dutta, and A. Terzis. Low Power or High Performance? A Tradeoff Whose Time Has Come (and Nearly Gone). pages 98–114, 2012.

[26] S. S. Kudva and R. Harjani. Fully-Integrated On-Chip DC-DC Converter With a 450X Output Range. *IEEE Journal of Solid-State Circuits (JSSC)*, 46(8):1940–1951, Aug 2011.

[27] J.-S. Lai and F. Z. Peng. Multilevel converters-a new breed of power converters. *Industry Applications, IEEE Transactions on*, 32(3):509–517, 1996.

[28] H.-P. Le, J. Crossley, S. Sanders, and E. Alon. A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm2 at 73% efficiency. *Int'l Solid-State Circuits Conf. (ISSCC)*, pages 372–373, 2013.

[29] H.-P. Le, S. R. Sanders, and E. Alon. Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters. *IEEE Journal of Solid-State Circuits (JSSC)*, 46(9):2120–2131, Sep 2011.

[30] J. Lee and N. S. Kim. Optimizing Throughput of Power- and Thermal-Constrained Multicore Processors using DVFS and Per-Core Power-Gating. *Design Automation Conf. (DAC)*, Jul 2009.

[31] H. Li, C.-Y. Cher, T. Vijaykumar, and R. K. VSV: L2- miss-driven variable supply-voltage scaling for low power. *Int'l Symp. on Microarchitecture (MICRO)*, pages 19–28, Jan 2003.

[32] D. Lo and C. Kozyrakis. Dynamic Management of TurboMode in Modern Multi-core Chips. *Int'l Symp. on High-Performance Computer Architecture (HPCA)*, Feb 2014.

[33] A. J. Martinez, A. A. Bajwa, D. L. Hill, E. Hallnor, H. Jiang, M. Dixon, M. Derr, M. Hunsaker, R. Kumar, R. B. Osborne, R. Rajwar, R. Singhal, R. D'Sa, R. Chappell, S. Kaushik, S. Chennupaty, S. Jourdan, S. Gunther, T. Piazza, and T. D. K. Burton. Haswell: The Fourth-Generation Intel Core Processor. *IEEE Micro*, 34(2):6–20, Mar/Apr 2014.

[34] R. Miftakhutdinov. An Analytical Comparison of Alternative Control Techniques for Powering Next-Generation Microprocessors. 2005.

[35] T. N. Miller, X. Pan, R. Thomas, N. Sedaghati, and R. Teodorescu. Booster: Reactive core acceleration for mitigating the effects of process variation and application imbalance in low-voltage chips. *Int'l Symp. on High-Performance Computer Architecture (HPCA)*, pages 1–12, Feb 2012.

[36] J. Park, D. Shin, N. Chang, and M. Pedram. Accurate modeling and calculation of delay and energy overheads of dynamic voltage scaling in modern high-performance microprocessors. *Int'l Symp. on Low-Power Electronics and Design (ISLPED)*, pages 419–424, Aug 2010.

[37] R. Pilawa-Podgurski and D. Perreault. Merged Two-Stage Power Converter With Soft Charging Switched-Capacitor Stage in 180 nm CMOS. *IEEE Journal of Solid-State Circuits*, 47(7):1557 –1567, Jul 2012.

[38] N. Pinckney, R. Dreslinski, K. Sewell, D. Fick, T. Mudge, D. Sylvester, and D. Blaauw. Limits of Parallelism and Boosting in Dim Silicon. *IEEE Micro*, 33(5):30–37, Sep/Oct 2013.

[39] A. Raghavan, L. Emurian, L. Shao, M. Papaefthymiou, K. Pipe, T. Wenisch, and M. Martin. Utilizing Dark Silicon to Save Energy with Computational Sprinting. *IEEE Micro*, 33(5):20–28, Sep/Oct 2013.

[40] Y. Ramadass, A. Fayed, and A. Chandrakasan. A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS. *IEEE Journal of Solid-State Circuits (JSSC)*, 45(12):2557–2565, 2010.

[41] V. Reddi, M. Gupta, G. Holloway, G.-Y. Wei, M. Smith, and D. Brooks. Voltage Emergency Prediction: Using Signatures to Reduce Operating Margins. *Int'l Symp. on High-Performance Computer Architecture (HPCA)*, 2009.

[42] S. Sanders, E. Alon, H.-P. Le, M. Seeman, M. John, and V. Ng. The Road to Fully Integrated DC-DC Conversion via the Switched-Capacitor Approach. *IEEE Transactions on Power Electronics*, 28:4146–4155, Sep 2013.

[43] M. Seeman. *A Design Methodology for Switched-Capacitor DC-DC Converters*. PhD thesis, EECS Department, University of California, Berkeley, 2009.

[44] M. Seeman, V. Ng, H.-P. Le, M. John, E. Alon, and S. Sanders. A comparative analysis of Switched-Capacitor and inductor-based DC-DC conversion technologies. *Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–7, 2010.

[45] N. Sturcken, M. Petracca, S. Warren, L. Carloni, A. Peterchev, and K. Shepard. An integrated four-phase buck converter delivering 1A/mm2 with 700ps controller delay and network-on-chip load in 45-nm SOI. *Custom Integrated Circuits Conf. (CICC)*, pages 1–4, 2011.

[46] O. Trescases and Y. Wen. A survey of light-load efficiency improvement techniques for low-power dc-dc converters. *Power Electronics and ECCE Asia (ICPE ECCE), 2011 IEEE 8th International Conference on*, pages 326–333, May 2011.

[47] D. Truong, W. Cheng, T. Mohsenin, Z. Yu, A. Jacobson, G. Landge, M. Meeuwsen, C. Watnik, A. Tran, Z. Xiao, E. Work, J. Webb, P. Mejia, and B. Baas. A 167-Processor Computational Platform in 65 nm CMOS. *IEEE Journal of Solid-State Circuits (JSSC)*, 44(4):1130–1144, Apr 2009.

[48] T. Van Breussegem and M. Steyaert. A fully integrated gearbox capacitive DC/DC-converter in 90nm CMOS: Optimization, control and measurements. pages 1–5, Jun 2010. 00007.

[49] G. Villar and E. Alarcon. Monolithic integration of a 3-level DCM-operated low-floating-capacitor buck converter for DC-DC step-down donversion in standard CMOS. pages 4229–4235, 2008. Cited by 0018.

[50] G. Villar and E. Alarcon. CMOS integrated switching power converters a structured design approach. 2011.

[51] G. Villar-Pique, H. Bergveld, and E. Alarcon. Survey and Benchmark of Fully Integrated Switching Power Converters: Switched-Capacitor Versus Inductive Approach. *IEEE Transactions on Power Electronics*, 28(9):4156–4167, Sep 2013.

[52] M. Wens and M. Steyaert. A Fully-Integrated CMOS 800-mW 4-Phase Semi-Constant On/Off-time Step-Down Converter. *IEEE Trans. on Power Electronics (TPEL)*, 26(2):326–333, Feb 2011.

[53] J. Wibben and R. Harjani. A High-Efficiency DCDC Converter Using 2 nH Integrated Inductors. *IEEE Journal of Solid-State Circuits (JSSC)*, 43(4):844–854, 2008.

[54] V. Yousefzadeh, E. Alarcon, and D. Maksimovic. Three-level buck converter for envelope tracking applications. *Power Electronics, IEEE Transactions on*, 21(2):549–552, 2006.

[55] F. Zhang, F. Peng, and Z. Qian. Study of the multilevel converters in DC-DC applications. 2:1702–1706 Vol.2, 2004.